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Circuit Techniques for the Design of Power-Efficient Radio Receivers

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Circuit Techniques for the Design of Power-Efficient Radio Receivers

by

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DISSERTATION

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY

THE UNIVERSITY OF TEXAS AT AUSTIN

December 2010

To

My beloved family, friends and teachers whom I look up to for inspiration

Acknowledgments

I would like to express my gratitude to the numerous people who have helped me reach this day. They are: Prof. Ranjit Gharpurey, for his infectious enthusiasm in working incessantly on problems trying to find elegant yet rigorous solutions, for all his advices, drive for perfection, teaching great courses, and standing by me encouraging when I needed the most. I would like to thank Dr. Stewart Taylor for his mentoring, agreeing to be on my committee and giving some simple yet profound advices about scientific pursuit which I hope to carry forward throughout my career. Prof. Adnan Aziz ensured I get an M.S. without financial worries. I want to thank him for being so nice to me - not just for being a committee member. I am extremely grateful to Prof. Michael Orshansky and Prof. Jacob Abraham for taking time out of their busy schedule and agreeing to be on my defense committee.

Some Professors who used to provide inspiration at Jadavpur University also need mention since they too helped shape me as a person just like the others whom I wanted to acknowledge. They are: Prof. *Debidas Mukhopadhyay* who with his unique teaching style managed to excite interest in device physics among many; Prof. Mrinal Kanti Naskar for his teaching and the image he portrayed in classes.

In course of my industrial job and internships at Texas Instruments (TI)

and Intel, I have been lucky to get help, mentoring and much needed (often implicit) encouragement from the following people: Reza, Rajarshi, Mark, Mike and Bryan (TI); Jon, Chang-Tsung, Stefano, Reggie and Rajesh (Intel); Uttam, Anand and Nitesh (TI, India). I want to thank them for whatever I could accomplish at those places. Those precious learning experiences did affect my contributions at school too.

Melissa, Debi and Andrew (specifically for his round-the-clock email replies) made CERC a great place to carry on work smoothly while forgetting about form-filling deadlines and the likes. Melanie inspires me for who she is and I consider myself extremely lucky to get help from such a role model for graduate advisor. Thanks also to Mary at ENS who helped ensure that my cries for keeping a decade old cadence license still working are taken care of.

I had a set of very friendly co-workers in Prof.'s research group with whom I interacted over time and the discussions were truly enjoyable. They are: Sungmin, Junghwan, Xin, Jaegan, Daniel, Wei, Jingxue, Wei Chi, Saurabh, Sahar, Shatam and Ashish. Many of them have also assisted me in completing my work, sometimes by helping out on items which are important but tedious to look around and get information on.

I am fortunate to have a diverse set of friends outside work who, despite their busy schedule and ignoring the fact that I hardly keep in regular touch, have always stepped up to any occasion I needed a help, not to mention the faith they had in me in the face of many setbacks. They are: from Austin

- Karthik, Gaurav, Vivek, Mayank, Vasu, Samaresh da, Amit, Chaoming, Rudrajit and Aniket; from the days at Jadavpur - Soumya, Satyabrata, Samik, Debdayal, Ananda da, Biman da, Soujanya and Pinaki da; from school and childhood days - Chitrak, *Subhankar*, Samrat and others.

People say last is not the least and I cannot reinforce that enough. I want to thank Maa for her unconditional love, patience and sacrifices to see me achieve my ambitions; *Baba*, who would have been proud to see this day, for teaching science and importantly a set of values he felt are worth possessing; Esha for her liveliness which makes India trips something I look forward to; Didi and Indranil da for their constant help, support and quietness when required.

This research was partially supported by a grant from the National Science Foundation (NSF Grant #ECCS 0824250). The views expressed herein do not necessarily reflect the views, position, or endorsement of the NSF. Research support of Texas Instruments Incorporated and chip fabrication support through the TSMC University Shuttle Program for our work on the quadrature receiver described in this dissertation is gratefully acknowledged.

Circuit Techniques for the Design of Power-Efficient Radio Receivers

Publication No. _____

Diptendu Ghosh, Ph.D.
The University of Texas at Austin, 2010

Supervisor: Ranjit Gharpurey

The demand for low power wireless transceiver implementations has been fueled by multiple applications in the recent decades, including cellular systems, wireless local area networks, personal area networks, biotelemetry and sensor networks. Dynamic range, which is set by linearity and sensitivity performance, is a critical design metric in many of these systems. Both linearity and sensitivity requirements continue to become progressively challenging in many systems due to greater spectrum usage and the need for high data rates respectively. The objective of this research is to investigate power-efficient circuit techniques for reducing the power requirement in receiver front-ends without compromising the dynamic range performance.

In the first part of the dissertation, a low power receiver down-converter topology for enhancing dynamic range performance is presented. Current mode down-converters with passive mixer cores have been shown to provide

excellent dynamic range performance. However, in contrast to a current-commutating Gilbert cell, these down-converters require separate bias current paths for the RF transconductor and the baseband transimpedance amplifier. The proposed topology reduces the power requirement of conventional current mode passive down-converter by sharing the bias current between the transconductance and transimpedance stages. This is achieved without compromising the available voltage headroom for either stage, which is a limitation of bias-sharing based on the use of stacked stages. The dynamic range of the basic bias-current-shared topology is further enhanced through suppression of low frequency noise and IM3 products. Two variants of the down-converter, employing a broadband common-gate and a narrowband common-source input stage, are implemented in a 0.18-μm CMOS technology. The dynamic range performance of the architecture is analyzed. Finally, a prototype of a full direct-conversion receiver implementation with quadrature outputs and integrated LO synthesis is demonstrated.

A power-efficient oscillator design for phase noise minimization is presented in the second part of this dissertation. This design is targeted towards multi-radio platforms where several communication links operate simultaneously over multiple frequency bands. Blockers from concurrently operating radios present a major design challenge. The blockers not only make the front-end linearity requirement more stringent but also degrade receiver sensitivity through reciprocal mixing with the phase noise sidebands of LO. Phase noise minimization is thus critical for ensuring high sensitivity in frequency bands

where large blockers are present and not sufficiently attenuated by pre-select filters.

A capacitive power combining technique in oscillators is introduced to improve phase noise performance. By combining this approach with current-reuse, the phase noise is reduced at lower power, compared to conventional LC oscillators. This leads to improved power efficiency. Moreover, the technique mitigates modeling uncertainty arising from phase noise reduction through simultaneous impedance and current scaling. The mode selection in this oscillator, which employs multiple coupled resonators, is analyzed and the impact of coupling on far-out phase noise performance is discussed.

Multi-mode oscillation can potentially arise in other oscillator topologies too, e.g., in multiphase oscillators. Mode selection in a widely used transistor-coupled quadrature oscillator is analyzed in detail in the final part of the dissertation. The analysis shows how cross-compression among multiple competing modes can lead to suppression of non-dominant modes in the steady state.

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Chapter 1

Introduction

The use of wireless technologies has become integral to modern life, with diverse end applications in communications, computing, healthcare and environmental monitoring. Specific examples of devices include cellphones, computers with integrated wireless connectivity, smart home appliances, personal area network devices for Bluetooth, GPS for location finding, transceivers for biotelemetry, and RF identification systems.

The use of Silicon technologies for high volume manufacturing has been an enabler for low-cost, highly integrated solutions for the above applications. CMOS technologies have allowed for the integration of analog and digital functionality on the same IC. The integration of discrete modules has facilitated low power operation, which is critical in many wireless applications, primarily by avoiding the requirement for power-hungry chip-to-board interfaces. A higher level of integration potentially also helps to reduce undesired coupling from spurious energy sources. Minimization of board components has also helped in reducing cost in several systems. Moreover, technological scaling has continued to push the limits of high frequency operation, thereby removing in many cases the requirement for the use of more expensive technologies.

This has helped serve the emerging needs of high data-rate communications, e.g., for real-time video transfer.

Technology scaling allows for greater digital functionality with enhanced power efficiency. It also allows for significant cost benefits from reduced area requirement. However, the decrease in voltage supply, which is a consequence of constant field scaling, poses a significant challenge for analog designs due to reduction in voltage headroom. A primary impact of reduced headroom is on linearity performance and the dynamic range of the RF front-end. Design and architectural solutions that enhance dynamic range performance in scaled technologies are therefore highly desirable, especially in energy-constrained applications, as discussed below.

1.1 System Evolution and the Need for Power-Efficient Radio Circuits

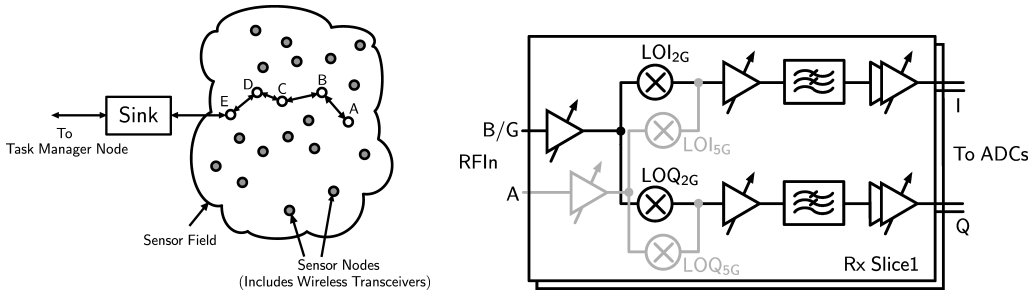
Requirements of current and emerging systems continue to place ever greater demands on dynamic range. The proliferation of wireless systems, and consequent greater use of spectrum further exacerbates the demands on linearity, due to the potential for greater interference, e.g., in the ISM bands at 2.4 GHz. Concurrently, the higher data rates supported in many systems through the use of higher-order modulation schemes, places greater requirements on sensitivity, and hence noise performance of the front-ends.

Dynamic range requirement, which is bounded by achievable linearity and sensitivity performance of transceivers, thus continues to become more se-

vere in many applications. When coupled with technology scaling as discussed previously, an increased dynamic range requirement poses an even greater design challenge.

A critical metric in energy constrained systems is the dynamic range per unit power. Maximizing this metric is highly desirable in many systems, for example in emerging WPAN applications like sensor networks (Fig. 1.1(a)). The basic units of such networks, called the sensor nodes, often work autonomously for monitoring, processing local data, communicating through peer-to-peer links and transmitting data to the internet gateway. Typically, these nodes have to work in hostile environments without supervision for years, and in some implementations rely on energy scavenging instead of batteries, which puts significant bounds on their operating power budget.

An extreme example of coexistence is observed in many current and emerging multi-mode, and multi-band cellular systems (Fig. 1.1(b)). In order to lower systems cost and provide single-chip solutions, many of these systems



(a) (b)

Figure 1.1: Wireless communication (a) Conceptual illustration of a wireless sensor network [1] (b) Receiver of a 2x2 multi-band MIMO transceiver for WLAN [2]

integrate multiple RF front-ends working across multiple standards and frequency bands, e.g., several contemporary smartphone models that are aimed to operate across several frequency bands (e.g., 7 bands spanning frequency 850 MHz to 2100 MHz, in WEDGE designs), and to allow simultaneous digital FM radio, Bluetooth, WiFi (802.11 b/g) and GPS connectivity [3]. Several of these radios are operational concurrently. This creates a significant coexistence issue and leads to an interference and blocker related dynamic range challenge.

In addition to limited energy constraints, e.g., battery life, there are also many instances in complex systems like above where trading power for increased dynamic range is not a feasible option, due to secondary considerations like thermal management. In such situations as well, increasing power efficiency is highly desirable.

This work addresses the problem of power efficiency in radio transceivers through circuit and architectural techniques. Specifically two key designs, a radio front-end and a power-efficient voltage controlled oscillator are addressed.

1.2 Organization

The dissertation is organized as follows. In Chapter 2, a brief review of receiver architectures, their key performance metrics and prior work on low power implementations are provided. Chapter 3 introduces a downconverter architecture for the purpose of dynamic range optimization. It utilizes techniques for bias sharing, noise suppression and intermodulation cancellation,

which are described. Measurement results for the downconverter implementations in a 0.18 μm CMOS technology are presented. In Chapter 4, a quadrature receiver employing a common source input stage is described along with the measurement results from its implementation. Prior work on phase noise minimization in power-efficient LC VCOs is briefly reviewed in Chapter 5. A VCO employing current reuse and capacitive coupling is introduced in Chapter 6. This section also includes a discussion of the design guidelines for suppressing multi-mode oscillation in the coupled resonator based oscillator topology and an analysis of the phase noise improvement under capacitive coupling in the in-phase coupled mode. Measurement results from a prototype implemented in 45 nm CMOS technology are presented. Chapter 7 presents a detailed analysis of oscillation growth in oscillators which can have multiple modes and discusses the how dominant mode can be selected by a natural process of cross-compression among competing modes in situations where they satisfy the startup criterion simultaneously. The contributions of this work are reviewed and scope for future research discussed in Chapter 8.

Chapter 2

Low Power Radio Receiver Design

The analog section of a modern radio receiver downconverts the signal detected by the antenna, and subsequently scales and band-limits the signal, so as to make it compatible with the dynamic range of the analog-to-digital converter (ADC), or the baseband detector. These processing tasks must be performed with minimal degradation of the received signal-to-noise ratio (SNR) so that the baseband performance metric, e.g., bit error rate (BER) is satisfied.

This chapter provides an overview of current state-of-the art radio receiver architectures. Key performance metrics are briefly discussed first. Currently employed topologies for minimizing power consumption in radio receivers are described subsequently.

2.1 Overview of Receiver Architectures and Metrics

2.1.1 Receiver Classification

Radio receiver architectures can be broadly classified based on whether the local oscillator (LO) frequency f_{LO} used for down-conversion is identical to or differs from the carrier frequency of the incident RF signal at f_{RF}. In

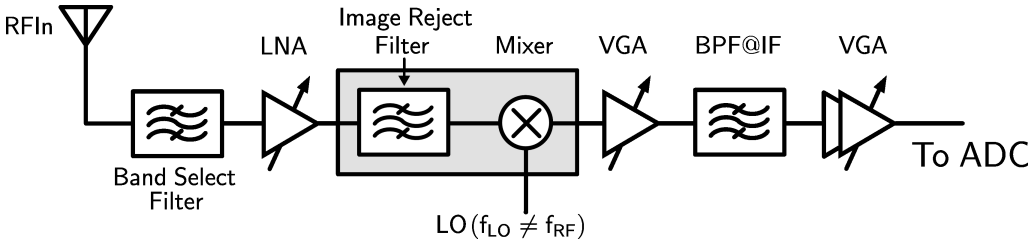


Figure 2.1: Single conversion heterodyne receiver

heterodyne receivers, the LO frequency is distinct from the RF carrier, while in direct downconversion receivers, the LO frequency is identical to the RF carrier. A heterodyne receiver can employ single or multiple intermediate frequencies (f_{IF}), before the signal is finally translated to baseband. For cases where f_{IF} is close to baseband, the architecture is often referred to as a low-IF receiver. Low-IF and direct downconversion receivers are integration friendly, and typically their entire front-end and baseband sections can be integrated on to a single IC, without the need for external filters.

Shown in Fig. 2.1 is a heterodyne receiver that employs a single IF. The RF signal received by the antenna is first applied to a band-pass filter. The signal band lies within the passband of the filter. The filtered signal is amplified by an RF amplifier (LNA). Before down-mixing, this amplified signal is applied to an image-reject filter which attenuates images located at $f_{RF} - 2f_{IF}$ (for upper sideband injection, i.e., $f_{RF} > f_{LO}$). The output of the mixer is applied to a cascade of low frequency variable-gain amplifiers and channel-select filters. The baseband signal may finally be digitized by an ADC. To meet stringent requirements imposed by standards like GSM, the image reject filter is often implemented off-chip using external passive elements. However, for re-

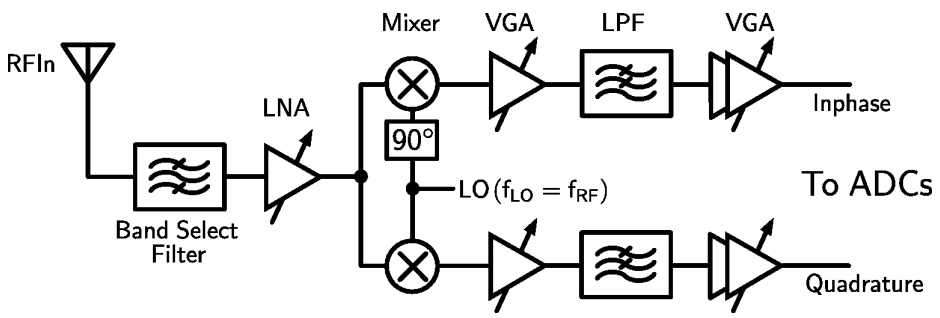


Figure 2.2: Direct conversion receiver

laxed specifications, power consumption can be minimized by using integrated complex filtering with the mixing operation. This approach is employed in Hartley and Weaver architectures. The complex filter in this case replaces the indicated circuit elements of Fig. 2.1.

To facilitate full-chip implementations without the need for image rejection, many contemporary receivers employ a direct-conversion approach as shown in Fig. 2.2. The RF front-end requires quadrature down-conversion since the carrier is not coherent in most implementations, with the received signal. The channel select filter is such cases is a low pass filter.

A direct conversion architecture, while very suitable for intergration, suffers from significant non-idealities that must be considered during design. These include DC offset generated by LO feedthrough into the RF port, degraded sensitivity due to $1/f$ noise, performance degradation due to second-order distortion which generates low frequency (in-band) spurious products, and SNR degradation due to I/Q mismatch. The use of calibration has been shown to be effective in mitigating several of these impairments.

2.1.2 Receiver Performance Metrics

The performance of a radio receiver is quantified by several important design metrics that are described here. A critical metric is the dynamic range, which as mentioned in Chapter 1, is determined by the difference between the linearity and sensitivity requirements.

Sensitivity is the smallest signal at the receiver input that is required to provide sufficient SNR at the output of the receiver, so that the baseband detector can perform satisfactorily. For digital modulation formats, satisfactory performance is measured by a minimum Bit Error Rate that the receiver must achieve. This sensitivity requirement places a bound on the noise performance of the receiver and is quantified by the Noise Figure (NF). The specification itself depends on several aspects of the communication protocol, such as modulation and coding. The Noise Figure is defined as the ratio of the SNR at the input of the receiver to the SNR at the output [4]. The achievable NF is determined strongly by the choice of architecture used for performing the signal processing and also the intrinsic device noise sources.

Often the received signal at the antenna is weak and has to be amplified to in order to make it commensurate with the dynamic range of the baseband detector or digitizer. The receiver conversion gain, defined at the voltage or power gain from the input at RF to the output at IF or baseband quantifies this. Due to the variation of the received energy, receivers typically require the gain to be dynamically adjusted in order to ensure that the detected SNR is not limited by either linearity for large input signals, or noise for weak input

signals. This requirement is specified by the variable gain range of the receiver. The gain range is usually partitioned across several variable-gain amplifiers for optimal control of the receiver performance.

The linearity is specified by several metrics which are determined by the level of of maximum tolerable intermodulation energy that can appear in-band without degrading the effective SNR by an unacceptable level. The key metrics that determine the non-linearity performance are the second-order and third-order intermodulation distortion products. These are quantified by the second and third-order input intercept points, IIP2 and IIP3, respectively [5]. Another important linearity metric, is the compression point, which is a measure of the input level require to reduce the small-signal gain of the receiver by a specified amount, such as 1-dB.

Non-idealities in the LO path also result in the degradation of SNR, e.g., the LO phase noise sidebands can beat with an adjacent channel blocker and introduce noise within the band of interest. In I-Q demodulation, the detected signal constellation can be corrupted by the mismatch in the amplitude and phase of the quadrature LO signals used for down-conversion. This makes oscillator phase noise and phase symmetry important design metrics.

Another key metric related to the frequency response of a receiver is its selectivity, which is defined as the ratio between the RF and channel frequency (f_{RF}/f_{CH}). The channel frequency or bandwidth (f_{CH}) is directly related to the data rate. Higher selectivity demands often impose severe design constraints in realizing a monolithic receiver implementation.

Impedance matching for maximizing power transfer into the receiver input from the antenna is often critical. The input reflection coefficient is often used to specify this requirement.

For a given receiver architecture, achieving sufficient dynamic range, gain and bandwidth sets the minimum power dissipation in the design. In many applications, especially where portability and mobility are essential, power dissipation is of paramount importance. Thus architectures that minimize power dissipation at a given performance level are highly desirable in such applications.

2.2 Power Minimization Techniques in Radio Receiver Circuits

Several power minimization as well as power constrained performance optimization techniques in receiver down-converters have been investigated previously. Some of these techniques are discussed below.

The Fig. 2.3 shows a classical Gilbert cell mixer [6] which is widely used as a down-converter in radios. The differential RF input (v_{RF}) is applied to devices $MN_{(1,2)}$ which operate as input transconductors. Their output current (i_{RF}) is commutated to baseband using a switching quad which consists of devices M_{NS1-4}. The resulting baseband current (i_{BB}) is converted to voltage using a resistive differential load ($2R_L$). This resistor, and the capacitor C_L implements a single-pole RC filter. The switching quad transistors are biased either in saturation (ON-state) or in cutoff (OFF-state). The headroom re-

quirement due to the vertically stacked transistors that need to operate in the high gain region, namely saturation in MOSFETs and the forward-active region in BJTs, and the load resistor, limits the maximum achievable conversion gain and also the achievable NF.

An approach to improve the power efficiency of a basic Gilbert cell is shown in Fig. 2.4(a). In this topology [7] part of the bias current through the NMOS input pair $MN_{(1,2)}$ is reused in the PMOS devices $MP_{(1,2)}$. AC-coupling of the RF input to the PMOS gates using C_{AC} increases the effective transconductance. Further, the reduced current flow though the load R_L lowers the static voltage drop through these. As such, the gain of the topology can be increased by scaling the resistors to a larger value than what is possible in a conventional Gilbert cell mixer. The reduction in DC through the switching pair also results in improved flicker noise performance of this downconverter.

Power dissipation in a down-converter can be reduced by scaling the supply voltage. One possible approach [8] can be arrived at by interchanging

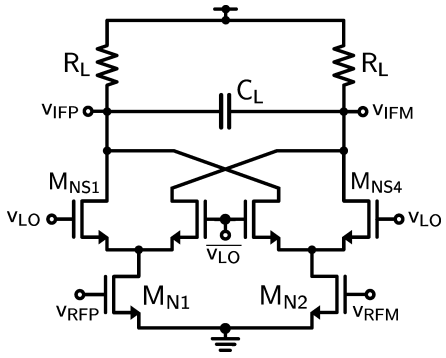


Figure 2.3: Gilbert cell mixer

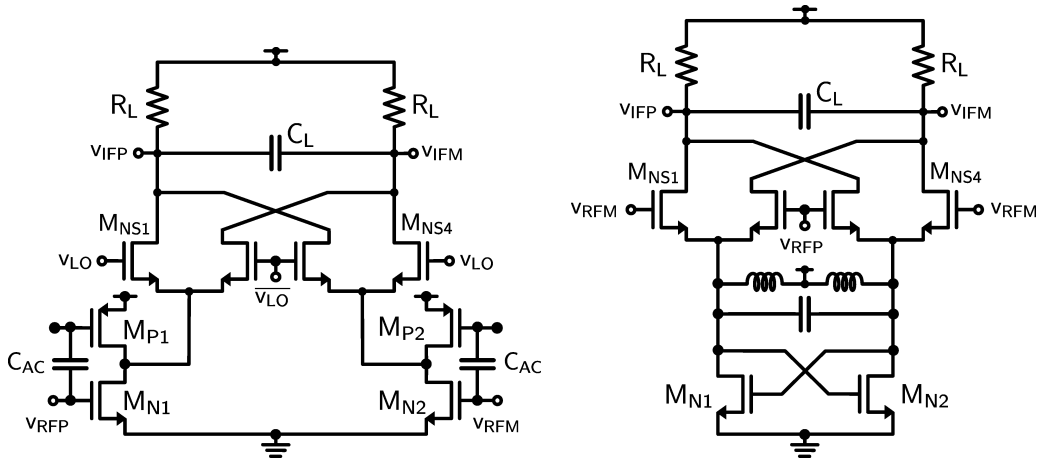


Figure 2.4: Downconversion mixer (a) Folded switching mixer (b) Merged mixer and oscillator

the RF and LO ports in the Fig. 2.4(a) and replacing C_{AC} by a short. The input devices $MN_{(1,2)}$ and $MP_{(1,2)}$ are then configured as LO buffers while M_{NS1-4} serve as switched transconductors. A variant of such topology [9] is shown in Fig. 2.4(b) where instead of an LO buffer, an LC oscillator is used to drive the source nodes of the devices M_{NS1-4} again operating as switched transconductors.

A different approach of current reuse was proposed in [10] for increasing the power efficiency significantly. The basic technique relied on the observation that any transconductance realized with a MOSFET is inherently broadband and can thus be reused for amplification across multiple bands. Fig. 2.5 shows a simplified schematic of this topology. The devices $MN_{(1,2)}$ convert the RF input voltage into current, which sees a low RF impedance looking into a

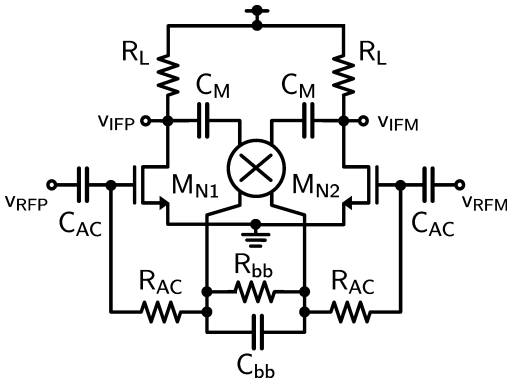


Figure 2.5: Mixer with multiband feedback

mixer core and subsequently gets down-converted to baseband. A network of passives R_{bb}, R_{AC}, C_{bb} and C_{AC} serves simultaneously as a baseband load and low pass filter. The resultant baseband voltage ($\propto g_{mn}R_{bb}v_{rf}$) appearing at the gates of $MN_{(1,2)}$, now acting as baseband transconductors, is subsequently reamplified by a factor $\propto g_{mn}R_L$ and extracted at baseband output.

In [11], the authors have presented an implementation of current reuse between an LNA, mixer and VCO. The core structure, which is referred to as double switching pair self-oscillating mixer, is shown in Fig. 2.6. RF signal is applied to a transconductor implemented by M_{NL}. The resulting RF current is commutated to baseband by the switching pair $M_{NM(1,2)}$ and converted to voltage by the load impedance presented by the IF Load. $M_{NM(1,2)}$ is driven by an LC-VCO, which is implemented using a cross-coupled pair. The cross-coupled pair is effectively pseudo-differential at baseband, due to the low impedance provided by the capacitor C_d. The VCO is stacked atop the switching devices. To reduce the impact of parasitic capacitance that appears

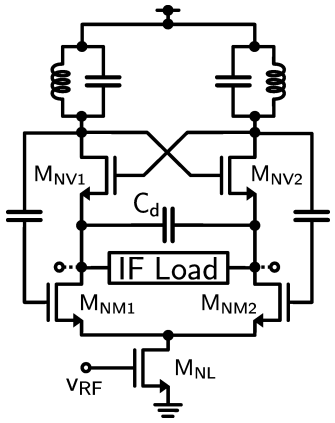


Figure 2.6: Double switching pair self-oscillating mixer

due to direct voltage sensing at the drain nodes of $M_{NM(1,2)}$, the IF Load is implemented as a transimpedance amplifier which performs current to voltage conversion at baseband.

In this chapter we reviewed some existing circuit techniques for enhancing power efficiency, e.g., through low voltage designs, re-use of components across multiple frequency bands or using stacked elements. In the next chapter we will present our proposed bias-current-shared receiver down-converter topology and discuss its unique attributes. Through the use of dynamic range enhancement techniques for reducing low frequency noise and non-linear products, and simultaneous voltage and current sharing, it is shown that this design achieves significantly higher power efficiency compared to prior art.

Chapter 3

Low Power Receiver Down-converters

3.1 Introduction

As mentioned in Chapter 1, receiver front-end architectures that enhance the achievable dynamic range per unit power dissipation are highly attractive for a wide range of wireless applications, including PAN, LAN and cellular systems, as well as emerging applications related to medical telemetry and monitoring.

In this chapter we describe a low power, dynamic range optimized down-converter topology for use in direct conversion or low-IF receivers. The design employs a current commutating passive mixer for frequency translation. This topology has been shown to possess excellent dynamic range performance ([12][13][14]). However, unlike typical implementations based on passive mixers, that use a distinct RF input transconductor stage and baseband amplifier with independent bias currents, the design described here shares the bias between the two stages, thereby reducing the power dissipation.

The RF transconductor in the two versions of the proposed topology consists of either a differential NMOS common-gate stage or a common-source stage which is power matched over a narrow bandwidth. The design with the

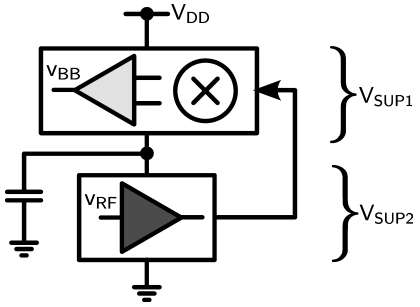


Figure 3.1: Conceptual implementation of stacked bias sharing

common-source input provides better sensitivity and greater conversion gain, at the expense of input-referred linearity. A baseband amplifier that employs PMOS common-source devices with shunt-shunt feedback is configured as a transimpedance stage. These devices also serve to bias the RF devices. The baseband stage presents a low input resistance at IF, and a high-impedance load to the RF input stage. The RF stage serves as a load to the transimpedance amplifier. A double-balanced current-commutating passive mixer is AC-coupled to the output of the RF transconductor and connected to the inputs of the baseband amplifier. Low-frequency (LF) noise and offsets are reduced by using an active suppression technique. Linearity performance is enhanced through the use of non-linear feedback at baseband. While the designs are intended for low power applications such as those in the ISM bands, their high dynamic range per unit power FOM [15] makes them suitable as power-efficient down-converters for more demanding systems such as cellular transceivers as well.

As described below, the topology is different from the current-reuse

technique reported in [11] which uses independent bias paths for current mode active mixer switches and transimpedance stage and from the approach of [7][16], where down-converters with stacked complementary transconductors which drive the mixer core are employed. A key differentiating aspect of the design is that unlike a stacked bias-sharing technique (e.g. Fig. 3.1), where the supply voltage is split across multiple stages, in this case the full supply voltage is available for both the baseband and RF stages, even through the bias is shared. The technique is also distinct from the architecture reported in [10] which exploits multiband feedback to increase dynamic range per unit power.

In Section 3.2, the operational principle of the down-converter and optimizations for noise and linearity are discussed in further detail. The conversion gain, noise and linearity of the down-converter are analyzed in Section 3.3. Experimental results are presented in Section 3.4. Tradeoffs between power and noise or linearity performance, as observed in simulation, is discussed briefly in Section 3.5. Conclusions are drawn in Section 3.6.

3.2 Principle of Operation and Design Implementation

3.2.1 Overview

Down-converters that employ passive CMOS current-mode mixers operate by commutating the RF current provided by an input transconductor. A low-impedance baseband termination is employed to minimize the voltage swing at the source and drain terminals of the on-state switches which en-

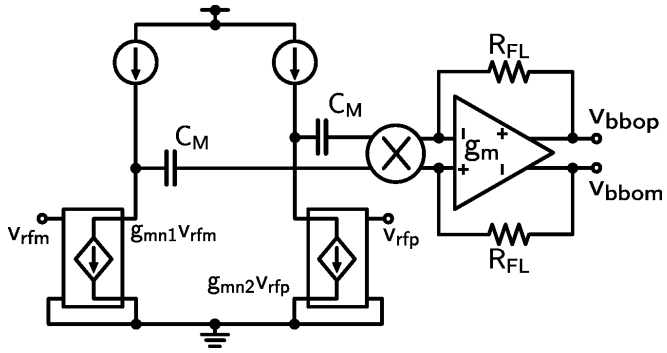


Figure 3.2: Conventional down-converter with passive current-mode mixer

sures higher linearity [14] compared to voltage-mode passive mixers. Since the switches operate with no DC, their flicker noise contribution is minimal. The flicker noise at the output is thus dominated by that of the baseband stage.

The RF transconductor and the baseband transimpedance amplifier typically use distinct bias paths in these designs. By contrast an active implementation, using a current-commutating Gilbert cell, utilizes the same bias current to accomplish the above tasks, although at the expense of higher flicker noise from the switches [17] and potentially higher non-linearity due to the significant voltage swing across the drain-to-source of the switching devices. The proposed down-converter topology shares the bias current for RF and baseband amplification while using circuit techniques described in the Subsections 3.2.4 and 3.2.5, to enhance the flicker noise corner and linearity of the design.

3.2.2 Bias-current-shared Topology

A conceptual diagram of a conventional down-converter with current mode passive mixer is shown in Fig. 3.2. The RF current from transconductors g_{mn1} and g_{mn2} is applied to an AC-coupled double-balanced switching mixer core. The passive mixer downconverts the RF currenr. The downconverted RF current is converted to a voltage in the baseband amplifier, since it is configured as a transimpedance stage. A typical transimpedance stage uses an OPAMP, or a transconductor, with resistive feedback. Independent bias currents are required in such a case for the RF and the baseband, as mentioned above.

The power dissipation in the architecture can be reduced in principle by sharing the bias current between the RF transconductor and the baseband transimpedance amplifier. It is important to ensure that the information-bearing signal that is processed by bias-shared circuit stages does not self-interfere, that is, the operation of each of the circuit stages is orthogonal. In theory, this orthogonality should be inherent in receiver applications that use bias-sharing between RF and baseband stages, since signals at RF and baseband occupy significantly different portions of the spectrum. In addition to frequency domain isolation, a bias-sharing approach that splits the supply voltage introduces additional orthogonality between RF and baseband, through the use of isolated supply domains for the two parts of the receiver. Splitting the supply (e.g. Fig. 3.1) however, reduces the headroom available per stage, thus reducing the dynamic range per stage. Thus even if the overall cur-

rent dissipation is reduced, the dynamic range per unit power-dissipation may not improve in an approach such as this. As we demonstrate below, through an appropriate topology, splitting the supply voltage is not required, that is RF and baseband signals can coexist within the same supply voltage domain, while sharing the bias current. The advantage of this approach, is that the full supply voltage can be made available to either stage, which sharing the bias current. This leads to significant enhancement in the available dynamic range.

The approach is shown in Fig. 3.3(a), wherein a high impedance active load is implemented using transconductors g_{mp1} and g_{mp2} with feedback resistors R_{FL}. These transconductors are also re-used as the baseband transimpedance stage of the down-converter. A passive switching mixer is AC-

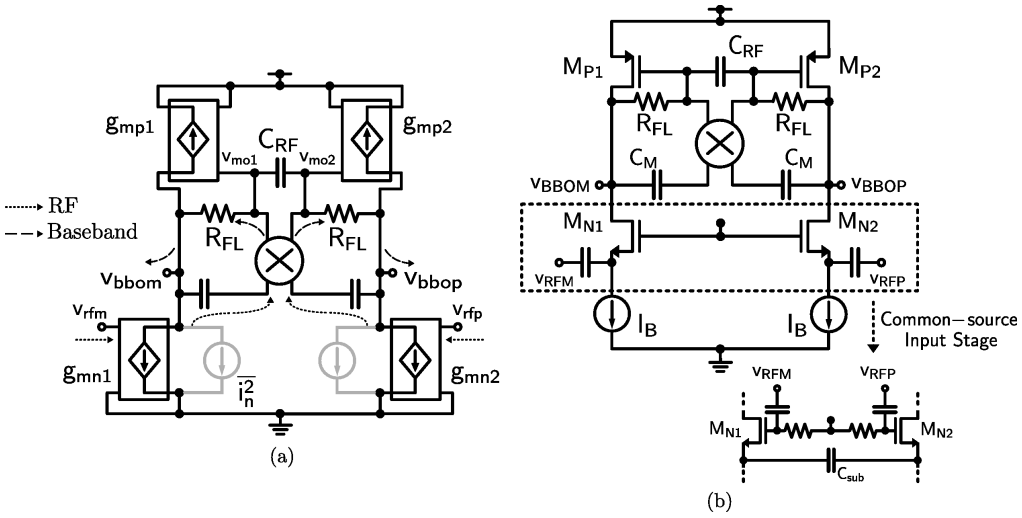


Figure 3.3: Bias-current-shared down-converter topology (a) Conceptual diagram (b) Basic implementation

coupled to the output of the RF transconductor through capacitors C_M and connected to the input of the baseband transimpedance stage.

A key role in this design is played by the capacitor (C_{RF}) which is connected differentially at the output of the mixer. This capacitor presents a low impedance at high frequencies, due to which the inputs of g_{mp1} and g_{mp2} are nearly shorted for differential signals at high frequencies. Consequently, the feedback through R_{FL} is effectively disabled at such frequencies. Thus for the differential high-frequency current at the output of the RF transconductor, a high impedance ($\sim 2R_{FL}$) is presented looking into the output nodes of g_{mp1} and g_{mp2}. The switching core of the mixer on the other hand, is designed to present a low impedance at RF due to which it acts as a current sink at RF. The origin of this low-impedance is described below. The RF current enters the switching core preferentially. It is downconverted to baseband and subsequently applied to the control inputs of the transconductors g_{mp1} and g_{mp2}. The capacitor (C_{RF}) presents a high impedance at the baseband frequency. Consequently, the feedback through R_{FL} across g_{mp1} and g_{mp2} is active and a low impedance of the order of $1/g_{mp}$ is observed at the control inputs. Thus the downconverted signal current is converted to a baseband voltage at the outputs of the transconductors g_{mp1} and g_{mp2}, which is also the differential output of the down-converter.

Fig. 3.3(b) shows a realization of the topology using a common-gate input stage. This type of input stage provides a broadband impedance match. The circuit operation at RF and baseband is illustrated in Fig. 3.4(a) and Fig.

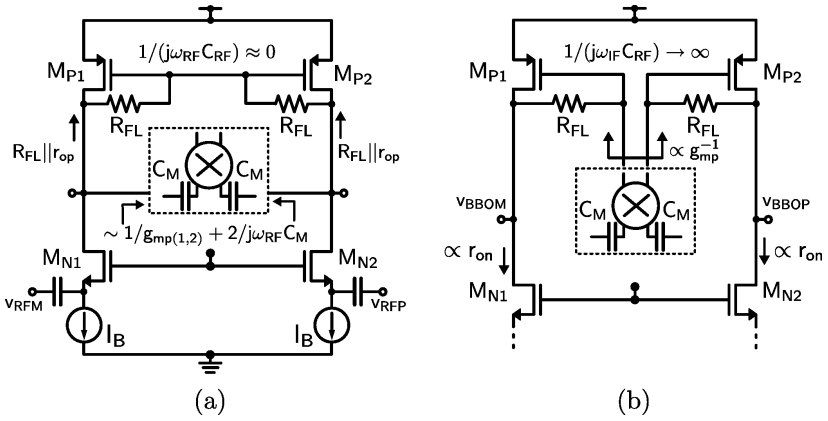


Figure 3.4: Differential signal flow in the basic bias-current-shared down-converter topology at (a) RF (b) Baseband

3.4(b) respectively. The RF and baseband stages each perform dual tasks. The devices M_{P1} and M_{P2} are used as baseband transimpedance amplifiers and also operate as high-impedance loads for the RF stage. The input devices M_{N1} and M_{N2} operate as RF transconductors while simultaneously providing a high-impedance load at baseband. As a consequence of this dual functionality, the RF and baseband stages share the available voltage headroom, while also sharing the bias current. Thus unlike a stacked bias-sharing approach, the supply voltage is not split across stages.

The topology reduces to a common-source input stage if the devices M_{N1} and M_{N2} are driven at their gates instead of their source nodes as shown in the Fig. 3.3(b). A capacitive short using C_{sub} between the source nodes of these devices makes the input transconductance stage fully differential at RF. Direct implementation of the topology shown in Fig. 3.3(a) also results in a common-source input stage. However, such a realization, as will be apparent

from our discussion shortly, leads to a degraded noise performance compared to the above common-source implementation.

3.2.3 Schematic Description

The schematic of the design with common-gate input is shown in Fig. 3.5. The input transconductor consists of a differential common-gate pair (M_{N1} and M_{N2}). Capacitive cross-coupling is utilized through capacitors C_g to increase the conversion gain and reduce noise figure [18]. The cross-coupling also ensures that the RF inputs are applied differentially across the gate-to-source of each of the input devices. The RF devices are terminated in active PMOS loads M_{P1} and M_{P2} that are biased using resistors R_{FX}. Due to the capacitor C_{RF} connected across the gates of M_{P1} and M_{P2}, these devices present a high-impedance differential load to the RF devices M_{N1} and M_{N2} given by $2(R_{FX} \mid\mid r_{op})$, where r_{op} is the PMOS small-signal output resistance.

For common-mode signals at any frequency, C_{RF} is floating. Thus for common-mode signals, M_{P1} and M_{P2} operate as common-source devices with shunt-shunt feedback, and provide a input low impedance of approximately $\{(R_{FX} + R_{bias})/R_{bias}\}(1/g_{mp(1,2)})$, which attenuates any common-mode component of the RF current.

A double-balanced switching mixer core consisting of NMOS switches M_{NS1-4} is AC-coupled through capacitors C_M to the drains of M_{N1} and M_{N2}. The switching core is connected at its output to the gates of M_{P1} and M_{P2}. Due to the feedback through R_{FX}, the low-frequency resistance

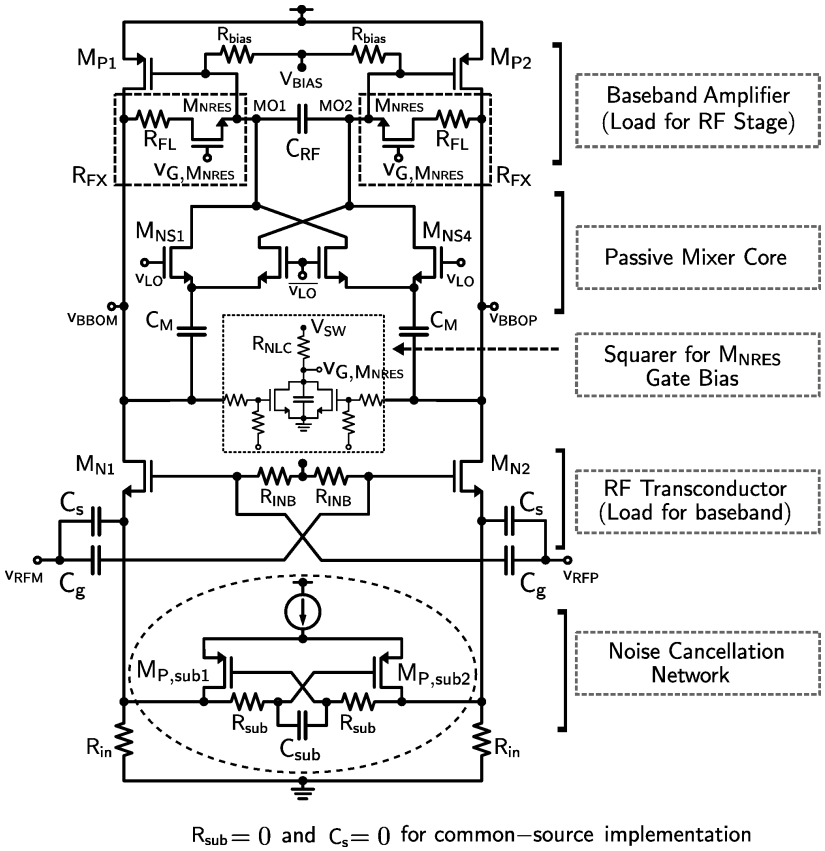


Figure 3.5: Schematic of the down-converter

looking into the gates of these devices is of the order of $(1/g_{mp(1,2)})||R_{bias}$. The low-frequency impedance is upconverted at the input of the mixer. Thus the differential impedance looking into the passive mixer is of the order of $(1/g_{mp(1,2)})||R_{bias}+2/\mathrm{j}\omega_{RF}C_M$ at RF, is significantly smaller than the differential impedance $2(R_{FX}||r_{op})$ looking into the drains of M_{P1} and M_{P2}. As a consequence, the RF current in M_{N1} and M_{N2} flows primarily into the mixer core. This is critical for ensuring that any parasitic capacitance at this node

does not attenuate the RF current flow into the mixer.[1] The low impedance termination provided by M_{P1} and M_{P2} at the outputs of the switches ensures current-mode operation. The switches commutate the RF current to baseband, which is filtered using C_{RF} and subsequently translated into a voltage at the drains of M_{P1} and M_{P2} through the resistance R_{FX}. Since the switches do not conduct DC, their flicker noise contribution is minimal.

The transistors M_{P1} and M_{P2} thus operate as pseudo-differential baseband amplifiers. The RF input pair M_{N1} and M_{N2} serves as a high impedance *load* for the baseband signals. The baseband signal is sensed at the drains of M_{N1} and M_{N2}. In the practical implementation, high-linearity unity-gain PMOS buffers with relatively high power were utilized to drive the external signals on board. These buffers are expected to be significantly smaller in an integrated receiver implementation, where the down-converter may be followed by an integrated filter or analog-to-digital converter. The differential LO is buffered on-chip using a cascade of two inverting buffers in our prototype.

3.2.4 Noise Suppression Network

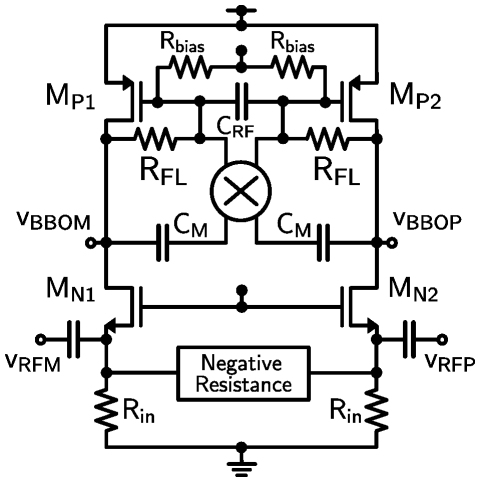
Since we employ direct conversion or low-IF operation, low-frequency noise at the output of the receiver is of significant concern. In the design of Fig. 3.2, any residual low-frequency noise at the input of the mixer core is upconverted and hence does not impact the downconverted signal. Additionally,

[1]The parasitic load at this node is similar in magnitude to that in a typical unfolded implementation, where a PMOS current source may be used to bias the NMOS transconductors.

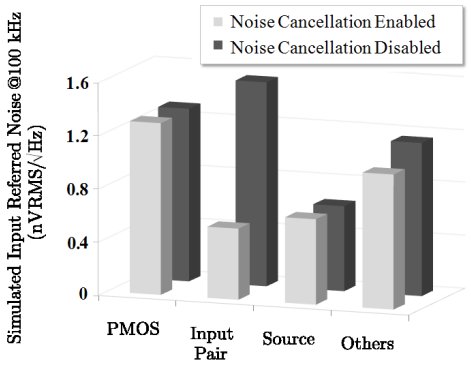
the RF stage is also typically AC coupled to the mixer, which further reduces the potential for its low-frequency noise entering the baseband stage. In the bias-current-shared topology (Fig. 3.3(a)) by contrast, the devices corresponding to RF transconductors $g_{mn(1,2)}$ are directly coupled to the baseband. A consequence of the direct coupling is that low-frequency noise and offsets in the RF transconductor appear at the output. As such, special design techniques are required to suppress this source of noise.

The RF devices are sized using the minimum channel length available in the technology, $L = 0.18\mu m$, to allow for high frequency operation and provide a high input transconductance. In addition to enhancing the high frequency gain, this also helps to reduce the input referred noise of the transimpedance stage. An undesirable consequence of theuse of short channel lengths for the RF devices, is that their flicker noise contribution can be large.

The design of Fig. 3.3(b), in principle, mitigates this noise contribution by utilizing an active source degeneration network consisting of the current source (I_B), which presents a high impedance at low frequencies, thereby attenuating the flicker noise of the input pair. However, if tail current sources employing NMOS transistors were used to bias the common-gate devices, then these would need to be made relatively large, in order to reduce their own flicker noise. This would lead to excessive parasitic capacitance, thus limiting the bandwidth at the input. To avoid this, while still reducing the flicker noise contribution of M_{N1} and M_{N2}, resistors R_{in} are used to bias the input devices in our implementation. However due to headroom constraints R_{in} can-



(a)



(b)

Figure 3.6: Noise suppression technique (a) Conceptual schematic (b) Representative partitioning of input referred noise in simulation

not be made arbitrarily large thereby limiting the achievable suppression of the low-frequency noise and intermodulation terms mentioned above.

The low-frequency differential-mode resistive degeneration is further enhanced without headroom or significant noise penalty, through the use of active negative resistance (Fig. 3.6(a)) in shunt with R_{in}, implemented using a cross-coupled PMOS pair $M_{P,sub(1,2)}$ employing devices biased in weak inversion. This results in a differential degeneration of $2R_{in}/(1 - g_{mp,sub}R_{in})$. The cross-coupled pair sees a low-frequency load of $2\{(1/g_{mn(1,2)})||R_{in}\}$, and is effectively shorted at high frequencies through C_{sub}.

The combined effect of C_{sub} and the low cut-off frequency of the weakly inverted devices $M_{P,sub(1,2)}$, ensures that the cross-coupled network is effective at baseband frequencies only and does not appear in the transfer func-

tion at RF. The differential input impedance seen at high frequencies by the signal source is thus approximately $(1/g_{mn(1,2)})||\{2(R_{in}||R_{sub})\}$. The resistor R_{sub}, however, is made much larger than R_{in} and thus the input impedance is approximately $1/g_{mn(1,2)}||(2R_{in})$. R_{sub} and C_{sub} help to ensure stability and broadband match simultaneously[2].

The flicker noise of the two input devices M_{N1} and M_{N2}, $i_{dn1,1/f}$ and $i_{dn2,1/f}$ respectively, can be expressed as a linear combination of differential and common-mode flicker noise terms as below.

$$i_{dn,1/f}^{diff} = i_{dn1,1/f} - i_{dn2,1/f} \tag{3.1}$$

$$i_{dn,1/f}^{comm} = (1/2)(i_{dn1,1/f} + i_{dn2,1/f}) \tag{3.2}$$

The resistive degeneration of the input devices provided by R_{in} decreases both the differential and common-mode terms at the output. The active cross-coupled network decreases only the differential mode noise $i_{dn,1/f}^{diff}$ at the output. The differential $1/f$ noise current is converted to a voltage by the differential low-frequency impedance observed looking into the drains of the PMOS devices. The capacitor C_{RF} is an open at low frequencies, and therefore the load devices M_{P1} and M_{P2} each present a low impedance ($\sim \{(R_{FX} + R_{bias}||R_{MIX})/R_{bias}||R_{MIX}\}(1/g_{mp1,2})$) at this frequency. R_{MIX} is an effective resistance between the gates of M_{P1} and M_{P2}. It arises predominantly

[2]It should be noted that the net resistance at the source nodes of the input devices $M_{N(1,2)}$ is guaranteed to be positive, since the cross-coupled devices $M_{P,sub(1,2)}$ have much lower g_m than the input devices.

from the parasitic capacitance at the mixer inputs, which is translated to an effective resistance at baseband, looking into the passive mixer from the gates of M_{P1} and M_{P2}. It appears in shunt with R_{bias}. The effect of R_{MIX} can be counteracted through design enhancements which we will discuss later.

The common-mode noise term $i_{dn,1/f}^{comm}$ is not attenuated by the cross-coupled network. However it is suppressed at the output by the low common-mode impedance presented by M_{P1} and M_{P2}. It is further suppressed by inherent common-mode rejection, since the outputs are observed differentially.

Finally, it is important to point out another impact of using the cross-coupled network. As described in Section 3.2.3, the RF devices M_{N1} and M_{N2} operate as loads for the PMOS transimpedance amplifiers. The differential degeneration provided by the cross-coupled pair at the source nodes of the RF devices significantly increases the output impedance at low frequencies, looking into the drains of M_{N1} and M_{N2}, which helps to increase the baseband gain.

The cross-coupled pair has practically no impact on linearity either at RF or baseband. As mentioned previously, the low-pass action of R_{sub} and C_{sub} effectively attenuates the RF signal at the gates of the cross-coupled pair. At baseband, the cross-coupled pair is isolated from the output nodes by M_{N1} and M_{N2}.

This design was intended to prototype the concepts presented above. As such the bias control of the cross-coupled pair was performed manually.

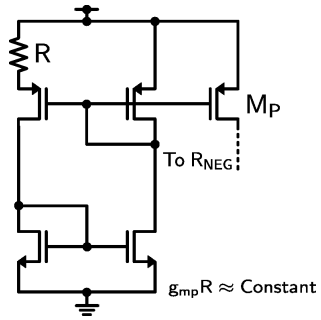


Figure 3.7: Constant $g_m R$ biasing

However, in principle, it is not difficult to implement an automated tracking scheme for setting this bias level, since the cross-coupled pair needs to have a fixed $g_{mp,sub}R_{in}$ product. A bias circuit that provides a constant $g_m R$ product [19] can easily be implemented (Fig. 3.7), to set the numerical value of this product close to one. As noted previously, even if the product exceeds 1, and the differential resistance provided by the combination of R_{in} and $1/g_{mp,sub}$ goes negative, the design is not unstable, since it is connected to a low-impedance set by the source of the input transistors ($\sim 2/g_{mn(1,2)}$) which is substantially smaller than $2/g_{mp,sub}$.

The simulated partitioning of the input referred noise for the down-converter is shown in Fig. 3.6(b). It is clearly seen that when the noise suppression network is enabled (curve marked "Noise Cancellation Enabled "), the noise from the input pair, i.e. devices M_{N1} and M_{N2} is significantly minimized.

Although in the above two sections we discussed the circuit implementation in the context of the down-converter with common-gate input stage,

the signal flow and the low frequency noise coupling mechanism are identical if a common-source input is employed. The schematic shown in Fig. 3.5 can be converted to a common-source input implementation by setting $C_s = 0$ and $R_{sub} = 0$. $C_s = 0$ implies that the external signal is applied only at the gates of M_{N1} and M_{N2}. While it may appear that for a common-source stage, a simple differential pair input stage with tail current source can be employed, doing so would cause the flicker noise of the input devices to appear at the output, just as above. Thus in this case too, degeneration provided by parallel combination of R_{in} and the active negative resistance suppresses the low frequency noise from input transistors M_{N1} and M_{N2}, similar to the common-gate design. C_{sub} plays the dual role of providing fully differential transconductor operation at RF, as well as making the cross-coupled network ineffective at RF. R_{sub} is not required as part of the baseband noise suppression network since C_{sub} does not impose input bandwidth limitation for the common-source input based design.

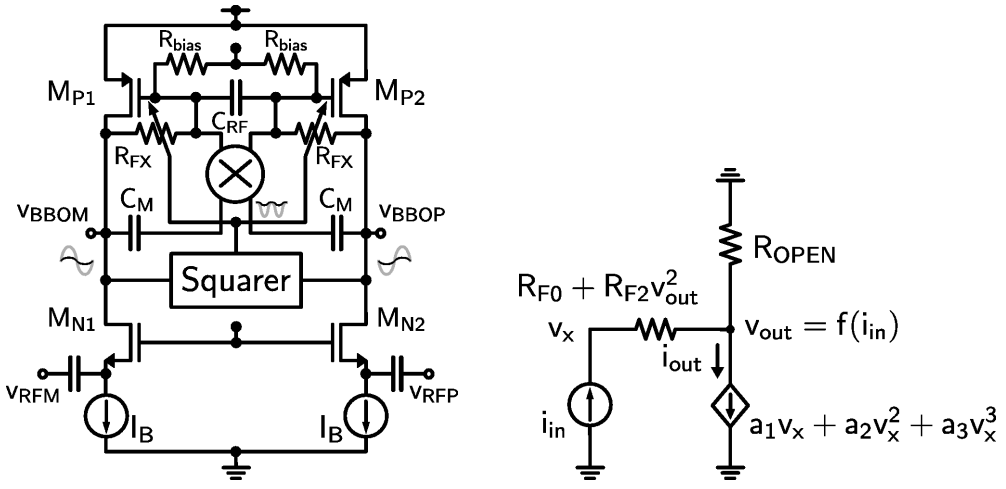
3.2.5 Linearity Enhancement Circuit

The linearity limitation in a down-converter incorporating passive current mode mixer typically arises from the RF transconductor and the baseband sections, since the switching core itself is very linear. The exact cause of key linearity limitations and the location in the signal chain where these can pose a design challenge, is system dependent. For example, in cellular systems such as W-CDMA, the 3^{rd}-order non-linearity is critical in the front-end, due to the potential for intermodulation with the transmitter signal. In a general

situation, however, linearity gets increasingly more challenging as we progress along the signal chain, since the signal is progressively amplified, and prior to baseband filtering, so are the interferers.

In this work, we specifically address the problem of baseband linearization. It is noted, that several very effective approaches have been presented in the past for the purpose of linearization of the RF stage [20][21], for example, derivative superposition [22], cascaded compensation of non-linear terms [23], and cancellation through injection of non-linear terms [24]. These techniques can also be studied in the context of the design reported here.

In our implementation we employ non-linear feedback for the purpose of baseband linearization. The technique realizes gain expansion in the transimpedance stage by using Voltage Controlled Resistors (VCR) (Fig. 3.8(a))



(a) (b)

Figure 3.8: Linearity enhancement technique (a) Conceptual schematic (b) Small signal single-ended model for baseband transimpedance stage

in the feedback path. The resistance of the VCRs is modified in response to the instantaneous amplitude of baseband output. The VCRs, denoted by R_{FX}, each consist of a series combination of a linear resistor R_{FL} and NMOS devices M_{NRES} biased in the triode-region. The non-linearity of the feedback is controlled by modulating the gate-bias of M_{NRES} using the outputs of a squarer circuit. The input of the squarer is DC-coupled to the baseband output of the down-converter through a high impedance resistive divider. This introduces a square-law voltage dependent term in the feedback resistor such that the resistance is increased as the amplitude increases. Modulation of the resistor provides gain expansion, which compensates for gain compression in the amplifier for large inputs. The technique is described in greater detail through the analysis given below. An significant feature of this technique for linearization is that it does not degrade noise, since the noise of the non-linear resistor M_{NRES} is identical to that of a linear resistor of the same nominal value. Further the magnitude of the non-linear resistor is typically considerably smaller than the linear resistor. A voltage V_{BIAS} fed through the resistors R_{bias} sets a stable DC voltage at the drains of M_{P1} and M_{P2}. The above linearity enhancement circuit is identical for both common-gate and common-source implementations.

3.3 Circuit Analysis

3.3.1 Overview

In this section we analyze the gain and noise performance of the proposed down-converter topology along with the working principle of the linearity enhancement technique. The analysis steps are detailed for the common-gate implementation while the results for the common-source implementation are summarized where relevant.

The capacitors, C_s, C_g, C_{sub}, C_M and C_{RF} (Fig. 3.5) are chosen to present a low impedance, ideally zero, at RF and a high impedance, ideally infinite, at baseband. The feedback resistance, R_{FX}, for the transimpedance amplifier is approximated as being equal to R_{FL} for gain and noise analysis. We assume that the passive mixer switches are ideal, i.e., r_{DS} of each switch is 0, when it is on, and approaches infinity when it is off. The output impedance of devices biased in saturation is ignored. The complementary LO signals are assumed to be square waves with 50% duty cycle.

3.3.2 Gain Analysis

The voltage conversion gain for the proposed topology (Fig. 3.5) can be evaluated by considering the signal flow through the down-converter (see Section 3.2.3).

The differential $v_{in} = v_{rfp} - v_{rfm}$ at RF is converted to differential RF current $i_{rf} = g_{mn}v_{in}$ by the input pair $M_{N1}$and M_{N2}. This expression includes the passive gain achieved by using cross-coupling capacitor C_g.

We denote the differential impedance looking into the passive mixer at RF as $Z_{in,mxr}(\omega_{RF})$. As derived in Appendix A, this impedance is significantly smaller compared to differential impedance presented looking into the drains of M_{P1} and M_{P2}, since at RF, the impedance of the capacitor C_{RF} is zero. Using the approximation that RF current flows entirely into the double-balanced switching core, the downconverted current at input of transimpedance amplifier is $i_{in} = (2/\pi)g_{mn}v_{in}$.

Applying KCL at the node $MO1$ (Fig. 3.5) we obtain,

$$i_{in} = \frac{v_{mo1}}{R_{bias}} + \frac{v_{mo1} - v_{bbom}}{R_{FL}} = \frac{v_{mo1}}{R_{bias}} + g_{mp}v_{mo1} \tag{3.3}$$

Solving for v_{bbom} and similarly v_{bbop}, the voltage gain from the differential input to differential output nodes of the down-converter can be shown to be

$$\frac{v_{bbop} - v_{bbom}}{v_{rfp} - v_{rfm}} = G_{CG} = -\frac{4}{\pi}g_{mn}\frac{g_{mp}R_{bias}}{1 + g_{mp}R_{bias}}(R_{FL} - \frac{1}{g_{mp}}) \tag{3.4}$$

The common-source implementation has a voltage gain of $G_{CG}/2$ from the gates of M_{N1} and M_{N2} to the differential output. The factor of 1/2 arises due to the absence of cross-coupling capacitors C_g.

It is noted that the above expression of voltage gain needs to be scaled by a factor, determined by input $L - C$ matching network parameters for the common-gate (CG) and common-source (CS) input designs, to evaluate conversion gain from signal source to output.

Table 3.1: Noise Attenuation Factors

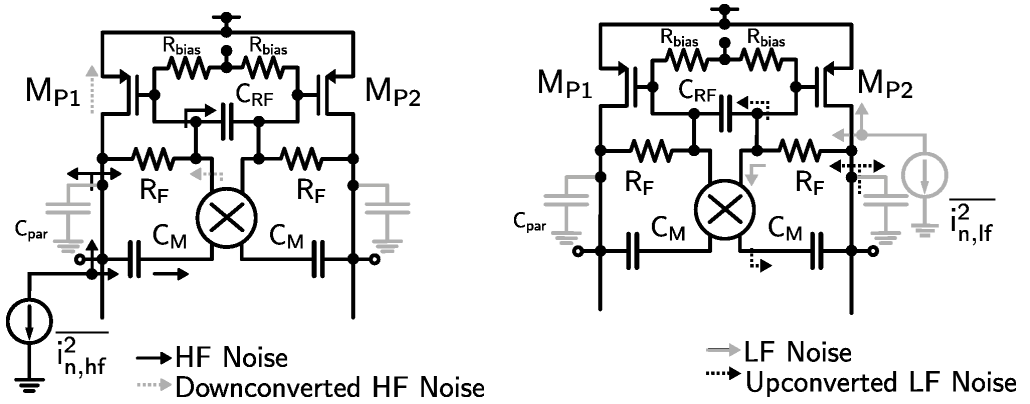
	$\kappa_{lf,MN}$	$\kappa_{hf,MN}$	$\kappa_{lf,MPsub}$	$\kappa_{hf,MPsub}$	$\kappa_{lf,MP}$	$\kappa_{hf,MP}$
CG	0	$\frac{1}{1+2g_{mn}R_s\|\|R_{in}\|\|R_{sub}}$	1	$\frac{R_s\|\|R_{in}\|\|R_{sub}}{1+2g_{mn}R_s\|\|R_{in}\|\|R_{sub}}$	1	1
CS	0	1	1	0	1	1

3.3.3 Noise Analysis

The dominant sources of noise at the down-converter output are the transistors $M_{N(1,2)}$, $M_{P(1,2)}$ and $M_{P,sub(1,2)}$. We perform the noise analysis through a two-step process as detailed below. Only the differential mode noise is considered since the common-mode components are suppressed due to differential observation of the signal at the output as mentioned earlier. The non-linearity cancellation loop is not considered in this analysis since it does not affect the noise performance of the down-converter. Subscripts "lf" and "hf" are used to denote low-frequency and high-frequency noise components respectively.

The drain current noise from each of the above devices, e.g. $i_{n,lf,MN}$ for M_{N1} and M_{N2}, is attenuated by different frequency-dependent factors, e.g. $\kappa_{lf,MN}$, due to the active noise suppression network at the sources of M_{N1} and M_{N2}. Table 3.1 lists the magnitude of these factors for the above noise sources in the CG and CS input implementations. It is assumed that the differential signal source resistance is $2R_s$, and $R_{in} = 1/g_{mp,sub}$.

The attenuated noise currents are injected into the time-varying switching core and are subsequently converted to baseband noise which appears at



(a) (b)

Figure 3.9: Current noise propagation through the switching core (Differentially symmetric paths not marked) (a) High frequency input noise (b) Low frequency input noise

the down-converter output. The propagation paths, within the switching core for high frequency noise at around odd harmonics of square wave LO are shown in Fig. 3.9(a). For estimating their noise transfer functions we denote that the differential impedance looking into mixer core at frequency $(n\omega_{LO}+\Delta\omega)$ to be $Z_{in,mxr}(n\omega_{LO}+\Delta\omega)$, where n is a positive integer. The fractional noise current flowing into the passive mixer at frequency $(n\omega_{LO}+\Delta\omega)$ due to injection at the down-converter output node is thus given by

$$\alpha_n \approx \frac{R_{FL}||\frac{1}{jn\omega_{LO}C_{par}}}{\frac{1}{2}Z_{in,mxr}(n\omega_{LO}+\Delta\omega)+R_{FL}||\frac{1}{jn\omega_{LO}C_{par}}} \tag{3.5}$$

where,

$$Z_{in,mxr}(n\omega_{LO}+\Delta\omega) \approx \frac{8}{n^2\pi^2}(\frac{1}{g_{mp}}||\frac{1}{\mathrm{j}\Delta\omega C})$$

R_{FL} is defined in the previous section and is the linear resistor in feedback

path of the transimpedance amplifier.

The conversion gain from high frequency current noise ($n\omega_{LO} + \Delta\omega$) to baseband output voltage at $\Delta\omega$ produced by beating with odd harmonics of ω_{LO} is given by

$$R_{conv,hf}(n\omega_{LO} + \Delta\omega) = (R_{FL} - \frac{1}{g_{mp}})\frac{g_{mp}R_{bias}}{1 + g_{mp}R_{bias}}\frac{\alpha_n}{n}\frac{2}{\pi} \tag{3.6}$$

for odd values of n. Since $\frac{1}{2}Z_{in,mxr}(n\omega_{LO} + \Delta\omega)$ is significantly lower than $R_{FL}||\frac{1}{jn\omega_{LO}C_{par}}$ (current mode operation), α_n can be approximated as unity.

Any low frequency current noise at $\Delta\omega$, injected at the down-converter output node appears as a voltage noise after propagating through the path illustrated in Fig. 3.9(b) with conversion gain given by

$$R_{conv,lf} = -\frac{R_{FL} + R_1}{1 + g_{mp}R_1} \tag{3.7}$$

where,

$$R_1 = R_{bias}||\frac{1}{4f_{LO}C_{par}}||R_{FL} \tag{3.8}$$

The expression for R_1 takes into account the impedance (R_{MIX}), which equals $(1/(4f_{LO}C_{par}))||R_{FL}$, at baseband looking back into the bilateral passive mixer core from the nodes $MO1$ and $MO2$. $1/(4f_{LO}C_{par})$ is the resistance of the switched capacitor resistor produced by C_{par} [25]. At RF, C_{RF} is nearly a short. Consequently, the impedance at RF looking back from the input of the passive mixer is given by R_{FL}, ignoring the output resistance of the PMOS and NMOS devices as mentioned previously. This impedance is translated in

frequency and presents an impedance of R_{FL} at baseband looking back into the mixer from its output and appears in shunt with $1/(4f_{LO}C_{par})$.

The total noise at the differential output for each implementation can be evaluated using the equations (3.6) through (3.8) and Table 2.1 as

$$\begin{aligned} N_{out}(f_{BB}) \approx 2[&(\overline{i^2_{n,lf,MP}}\kappa^2_{lf,MP} + \overline{i^2_{n,lf,MN}}\kappa^2_{lf,MN} + \overline{i^2_{n,lf,MPsub}}\kappa^2_{lf,MPsub})R^2_{conv,lf} \\ &+2(\overline{i^2_{n,hf,MP}}\kappa^2_{hf,MP} + \overline{i^2_{n,hf,MN}}\kappa^2_{hf,MN} + \overline{i^2_{n,hf,MPsub}}\kappa^2_{hf,MPsub}) \\ &\sum_{i=0}^{\infty} |R^2_{conv,hf}((2i+1)\omega_{LO})|] \end{aligned} \tag{3.9}$$

where for each transistor,

$$\overline{i^2_{n,lf}} = 4kT\gamma g_{d0}\Delta f + \frac{g_m^2 k_{1/f}}{WL\frac{\varepsilon_{ox}}{t_{ox}}}\frac{\Delta f}{f_{BB}} \text{ and } \overline{i^2_{n,hf}} = 4kT\gamma g_{d0}\Delta f.$$

The first factor of 2 in equation (3.9) accounts for the differentially paired devices whereas the second one takes into account the noise from symmetric sidebands about LO harmonics which fold onto baseband.

3.3.4 Analysis of Linearity Enhancement Circuit

We describe below the impact of non-linear feedback on the linearity performance of the baseband transimpedance stage. All sources of non-linearity are assumed to be weak and memoryless, and thus are expressed using a power series. The baseband current (i_{in}) is fed to the transimpedance stage which is modeled as a non-linear transconductor with power series coefficients $\{a_1, a_2, a_3\}$. In a MOSFET, a_1 corresponds to the transconductance g_m, while a_2 and a_3 are proportional to the higher order derivatives $\partial^2 i_D/\partial v^2_{GS}$ and

$\partial^3 i_D/\partial v_{GS}^3$ respectively. The non-linear feedback resistor can be considered to the first order to be of the form $R_{F0} + R_{FC}v_c$ where v_c is the external control voltage. In the implementation v_c is derived using a squarer (Fig. 3.8(a)), and hence, $v_c = Kv_{out}^2$. This implies second-order dependence of R_{FX} on v_{out} and we canthus express $R_{FX} = R_{F0}+R_{F2}v_{out}^2$. Fig. 3.8(b) shows the half-circuit for differential mode operation of the transimpedance stage. R_{OPEN} is assumed to be infinity for the analysis. Using this model, we can evaluate, as shown in Appendix B, the effective non-linear coefficients of the transimpedance stage, represented by $v_{out} = b_1 i_{in} + b_2 i_{in}^2 + b_3 i_{in}^3$, as

$$b_1 = -R_{F0} + \frac{1}{a_1} \tag{3.10}$$

$$b_2 = -\frac{a_2}{a_1^3} \tag{3.11}$$

$$b_3 = -\frac{a_3}{a_1^4} + \frac{2a_2^2}{a_1^5} - R_{F2}b_1^2 \tag{3.12}$$

From equation (3.12), it is seen that the addition of the square law term in the feedback resistor produce an additional term $R_{F2}b_1^2$ in b_3. This can be used to cancel the native non-linearity of the transconductors $M_{P(1,2)}$ expressed by a_3 by making b_3 zero. This can be achieved by controlling the effective value of R_{F2} by proper choice of the gain and polarity of the square law detector.

As derived in Appendix C, the non-linear feedback resistor parameters can be expressed in terms of the device parameters and bias as

$$R_{F0} = R_{FL} + R_{SW}$$

$$R_{F2} = \frac{G_{C,SQR} R_{SW}}{V_{GST}} \tag{3.13}$$

where R_{FL} is the magnitude of the linear feedback resistor, $R_{SW} = 1/(k_n \frac{W_{SW}}{L_{SW}} V_{GST})$ is the signal-independent part of MOS resistance, $G_{C,SQR}$ is the gain of the squarer. From the derivation it follows that under a fixed bias in the down-converter core, V_{GST} of the MOS resistor and hence R_{SW} can be controlled by varying the bias V_{SW} (Fig. 3.5). This makes the coefficient magnitude b_3 controllable. As noted earlier, typically, $R_{SW} \ll R_{FL}$ and thus non-linearity cancellation can be achieved with negligible impact on linear gain of the stage. This is validated from our measured performance. It is noted that the second order coefficient, b_2 gets cancelled in differential implementation when there is no mismatch.

We will now briefly discuss the device sizing optimization based on the above analysis.

3.3.5 Device Sizing for optimizing FOM

The devices comprising the input transconductor employ the minimum channel length, L_{min} in order to maximize the cut-off frequency and gain. The width of input transconductor is chosen to optimize the NF at a fixed bias current $I_{MN(1,2)}$. For small device width (W), g_m and the conversion gain is low and which degrades the NF. For large widths, the conversion gain and NF degrade due to greater capacitive shunting of the RF current in this implementation. The NF degradation for large device width is in part due to increased contribution from the transimpedance stage that arises from the

loading of the switched capacitor resistor created by C_{par} (Fig. 3.9(b)) as described in [25][12][14].

The PMOS transistors M_{P1} and M_{P2} that form the baseband transimpedance employ a channel length greater than L_{min} to reduce their flicker noise contribution. Increasing the W-L product of these devices however also increases C_{par}. As noted previously, this increase degrades the NF, which places an upper bound on the device area. This in turn limits the largest channel length that may be used due to constraints on the V_{GS} of the PMOS devices in this implementation.

The PMOS devices that comprise the cross-coupled pair in the degeneration network are also sized such that their channel length is much greater than L_{min} to minimize flicker noise. Their bias current ($I_{MPsub(1,2)}$) is significantly lower than the current through RF transconductors to in order to minimize power penalty. The device width under this power constraint is set to achieve a $g_{mp,sub}$ that is approximately equal to $1/R_{in}$. The lower limit on $I_{MPsub(1,2)}$ is set by mismatch-induced offset constraints. The value of R_{in} is decided based on a maximum headroom constraint for a given bias current. Biasing the PMOS transistors in subthreshold is possible since the voltage swing across their gate-source terminals is small at RF.

The sizing and bias of M_{NSQR}, M_{NRES} and R_{NLC} are chosen to achieve the desired IM3 cancellation.

The current-commutating switches within the core use the minimum

channel length L_{min}. The width of these devices is set by two constraints. The lower limit on W is set by the requirement to ensure that the ON-resistance is kept below an upper bound, so that the conversion gain is not degraded. The upper limit on the width of the switches is set by their impact on the capacitance C_{par} at down-converter output.

3.4 Experimental Results

The down-converters with common-gate and common-source input were implemented in a commercial 0.18-μm CMOS process. The ICs were housed in 48 pin TQFP packages and measured on FR4 printed circuit boards. The designs used external baluns for feeding RF and LO. A balun loss of 2.2 dB was measured at the operating frequency, using a dedicated test fixture consisting of two baluns connected back-to-back. The measured performance was corrected for this attenuation. The baseband output signal was measured by using PCB-mounted external op-amps operating in a unity gain differential-to-single ended configuration.

The measured input return loss (S_{11}) for the common-gate implementation was better than -10 dB from 750 MHz to 1200 MHz. The bondwires (L_{bondw}) and PCB traces (L_{trc}) along with the external AC-coupling capacitors (C_{AC}), as shown Fig. 3.10, provided tuning around 1 GHz. The common-source implementation was impedance matched using additional on board passive elements, $L_{match,CS}$ and $C_{match,CS}$, to achieve an $|S_{11}|$ better than -10 dB over 880 MHz to 925 MHz, which also helped to boost its gain compared to

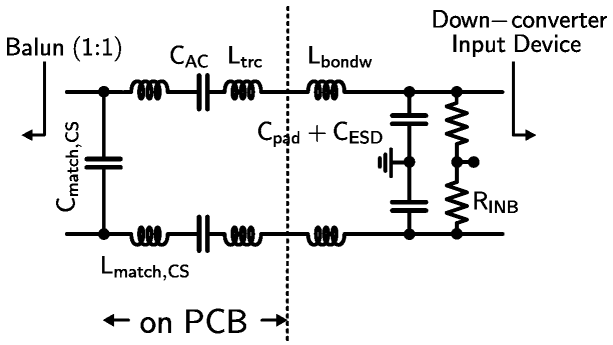


Figure 3.10: Input matching network for the down-converter

the common-gate design.

The measured conversion gain was 35 dB at 1 GHz for the CG in-

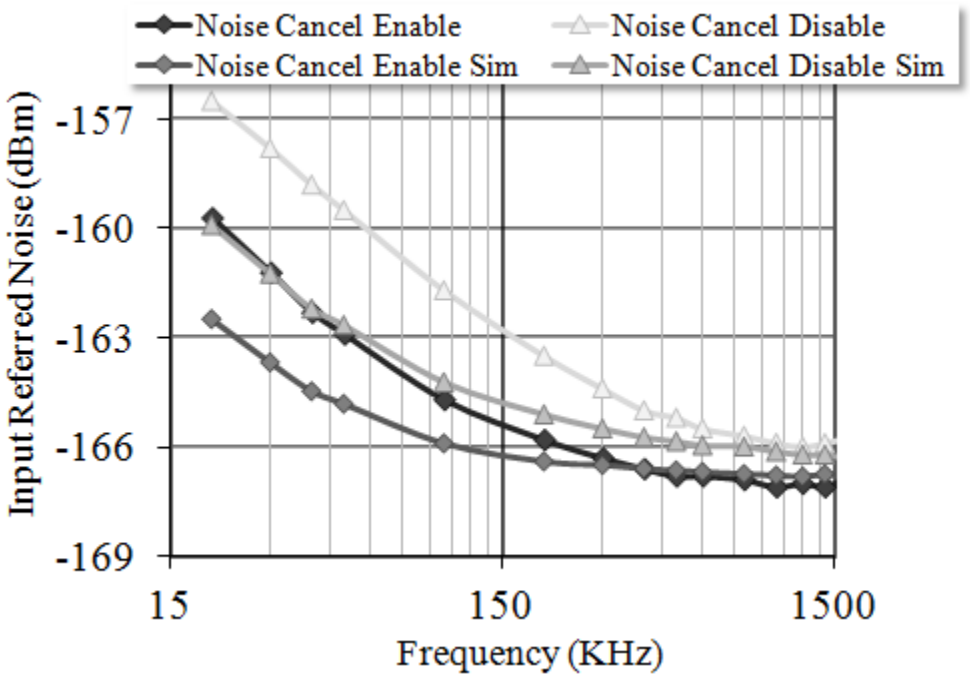


Figure 3.11: Common-source input down-converter noise variation for cross-coupled degeneration ON and OFF

put down-converter and 46 dB at 900 MHz for the CS input down-converter. The measured 3-dB bandwidth for both implementations was approximately 2 MHz. This bandwidth limitation arose from the loading by the capacitance of the cables and the PCB trace.

The double sideband noise figure (DSBNF) at 1 MHz IF was 9.8 dB for the CG and 3.9 dB for CS down-converter respectively. Fig. 3.11 shows the measured input referred noise for the CS input down-converter with and without the active noise suppression circuit. The curves labeled with suffix "Sim" correspond to simulated results. For both designs, the low frequency noise decreased by about 3-4 dB with the cross-coupled degeneration enabled

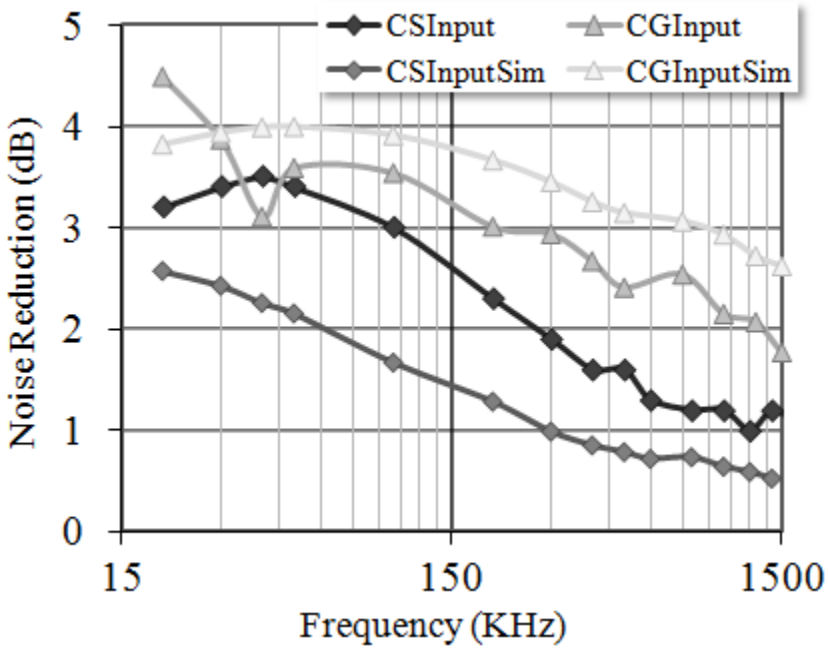


Figure 3.12: NF improvement achieved using noise suppression technique

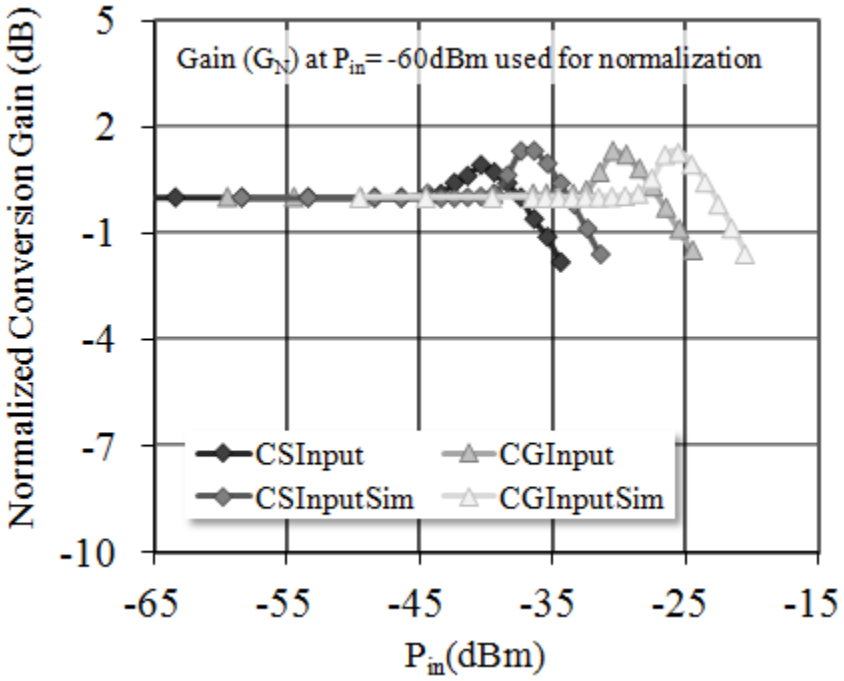


Figure 3.13: Measured gain compression plots

(Fig. 3.12). The dominant flicker noise contributors at baseband were the PMOS loads. These devices used a channel length of 0.24 μm in the design, which caused a relatively high flicker noise contribution. The resulting noise corner frequency was approximately 160 kHz (CG) and 85 kHz (CS). A possible approach to reduce the residual noise from the baseband PMOS devices will be demonstrated later in the context of our receiver implementation.

The in-channel 1-dB compression point is fundamentally set by the available voltage swing at the output nodes. Fig. 3.13 shows the normalized gain for the two implementations as a function of the input power (P_{in}). The 1-dB compression point was found to be nearly -1 dBVp at the output for

both designs, which implies an input compression of approximately -25 dBm and -36 dBm respectively for the CG and CS designs. The input P1dB can be increased by reducing R_{FL} to lower the gain or through incorporation of variable gain functionality as will be detailed in the next chapter.

The in-band IIP3, using tones at offset 400 kHz and 500 kHz from the LO at 1 GHz for the common-gate design was -9.2 dBm. The output IM3 demonstrates a 14 dB improvement with non-linearity cancellation. For the common-source design the IIP3 was -16.6 dBm (Fig. 3.14) and IM3 cancellation circuit was seen to reduce IM3 by 18.6 dB for two tones at similar offsets

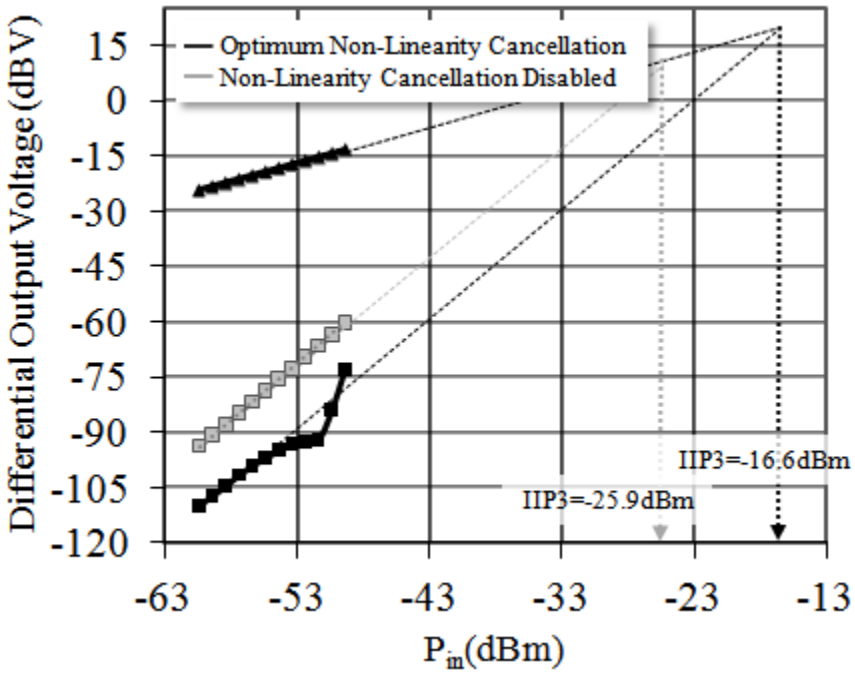


Figure 3.14: Common-source input down-converter IIP3 with and without non-linearity cancellation

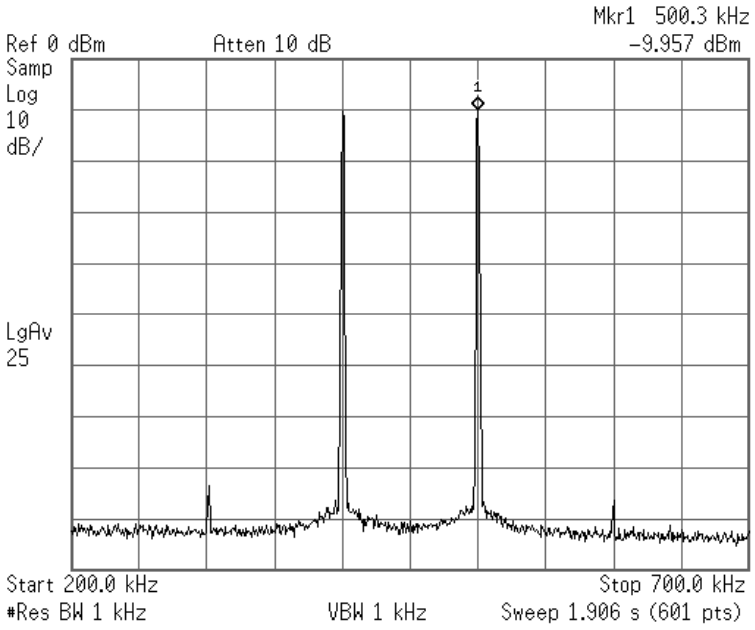


Figure 3.15: Measured common-source input down-converter output spectrum for two tone input

as above with LO at 900 MHz. A representative output spectrum for two tone excitation to the common-source design is shown in Fig. 3.15. The sensitivity of the linear and IM3 terms at the output to non-linearity cancellation bias is shown in Fig. 3.16 for both the designs. The deviations shown in the figure are relative to the linear and IM3 outputs obtained for a nominal $V_{GS,M_{NRES}}$ of approximately 0.78V. It can be observed that the IM3 is minimized ata distinct bias point . Furthermore, the linear gain changes minimally as a function of the bias point. As can be seen from the Fig. 3.11 through Fig. 3.16, there exists a general agreement in trends between measurement and simulation for the metrics determining the dynamic range performance of the down-converters.

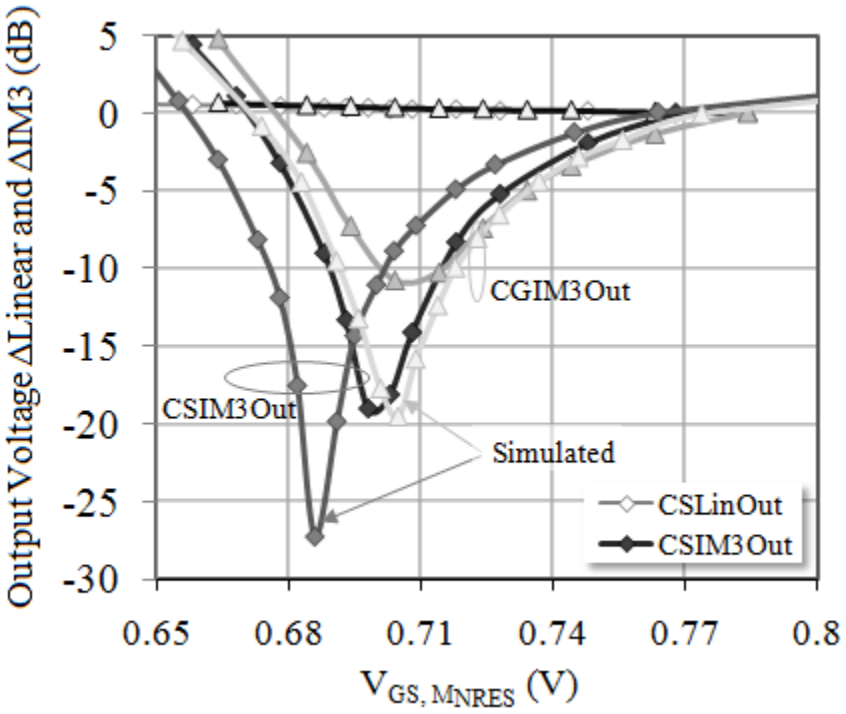


Figure 3.16: Measured variation of IM3 and linear output with gate bias of $M_{NRES(1,2)}$

The uncalibrated IIP2, measured using same tone frequencies as in the IIP3 test, was in the range 24 dBm to 28 dBm for both the designs. The impact of LO leakage was compensated in the measurement through an external LO injection to ensure accurate IM2 measurement. It is expected that the IIP2 performance for the down-converter can be significantly improved through calibration achieved by modifying the bias currents of the input devices to compensate for mismatches. However, a circuit for introducing bias tuning was not included in this design. A conceptual diagram for the setup used in the down-converter measurement is shown in Fig. 3.17.

The bias current requirement was 2.1 mA and 1.9 mA for the CG and CS designs respectively from a 1.8 V supply. The voltage bias for the buffered LO signal was chosen to optimize the noise and conversion gain performance. Each down-converter including the LO buffers had an area requirement of 0.2 mm^2. ESD protection was included in the design.

The calculated FOM [15] for the CG down-converter is 19 dB and for CS version is 27 dB. The die microphotograph is shown in Fig. 3.18. The measured performance metrics for our design and other reported implementations are compared in Table 3.2. The performance is seen to be better or comparable to other low power down-converter and receiver designs in similar technology nodes.

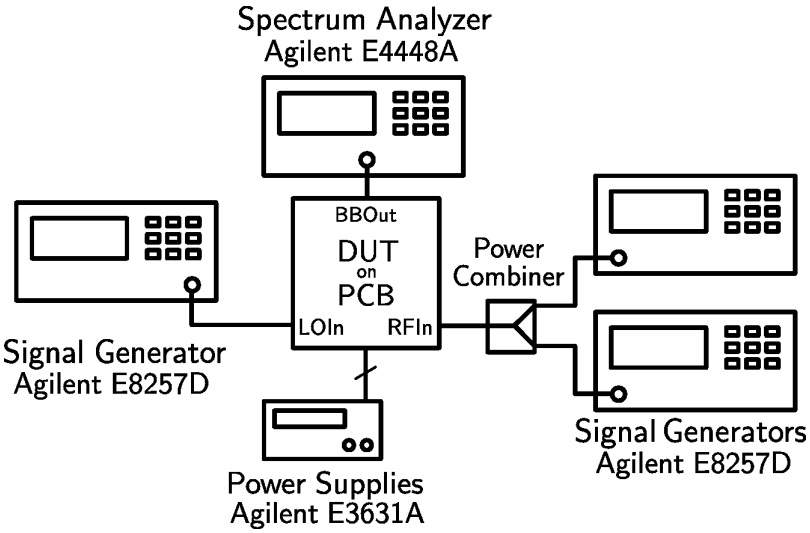


Figure 3.17: Down-converter measurement setup

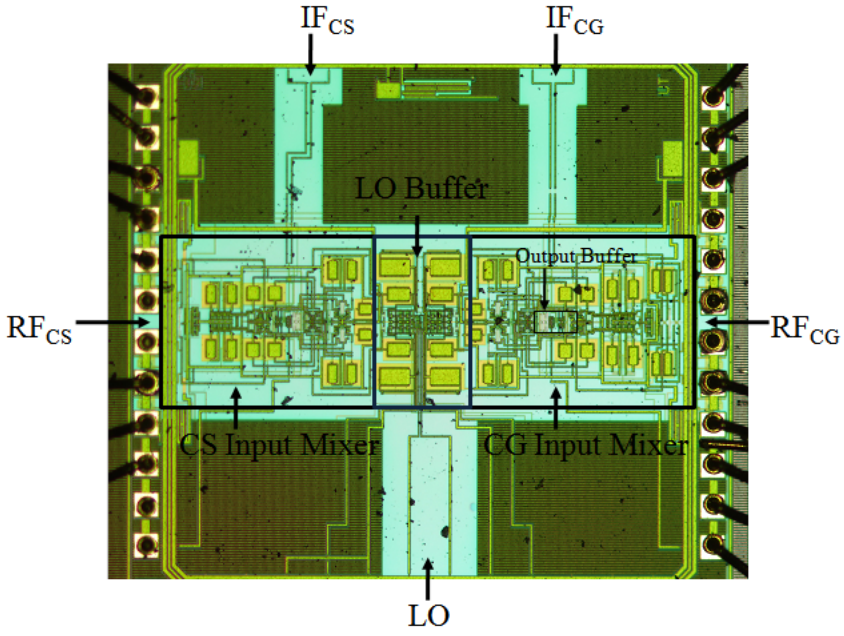


Figure 3.18: Die photograph

3.5 Tradeoff between Dynamic Range and Power

Although the architecture has been discussed in context of low power applications, re-optimizing the device parameters for higher power applications shows scope for increased dynamic range performance achievable from the topology. The representative simulated variation of noise figure, output 1-dB compression point and 3rd-order intercept points for the common-gate input down-converter are shown in Fig. 3.19, Fig. 3.20 and Fig. 3.21 respectively to demonstrate this tradeoff. As seen from Fig. 3.19, the noise figure decreases with increasing current irrespective of the supply voltage. The minor degradation of noise on increasing supply while keeping current fixed can potentially be due to degraded excess noise factor (γ) of the active devices working in ve-

locity saturated regions. The compression point is observed to degrade at high current levels. This is expected to be a result of reduced headroom available under these conditions. As mentioned earlier, in this design the compression point is predominantly limited by the output swing. This also explains its significant improvement on increasing supply voltage. The OIP3 improves with high current since it is a strong function of the gate-source overdrive of the RF input pair.

The FOM variation, for the common-gate design, in measurements at different supply voltages with optimally chosen bias but fixed device sizing is shown in Fig. 3.22.

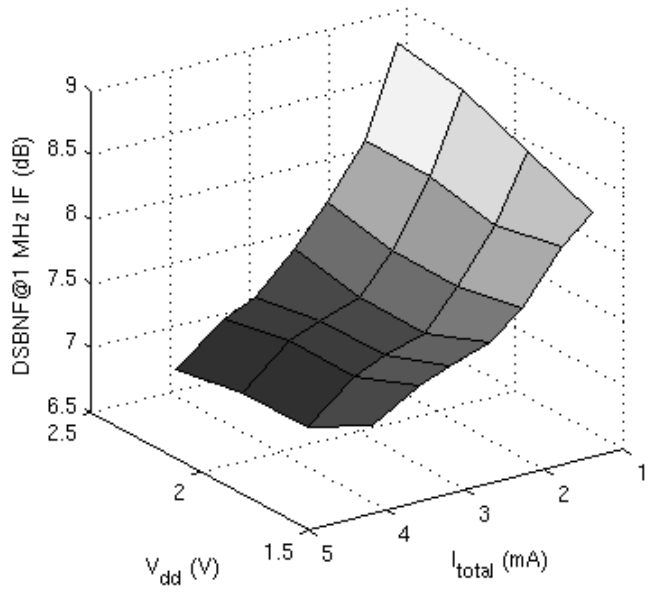


Figure 3.19: Simulated DSBNF of the common-gate input down-converter

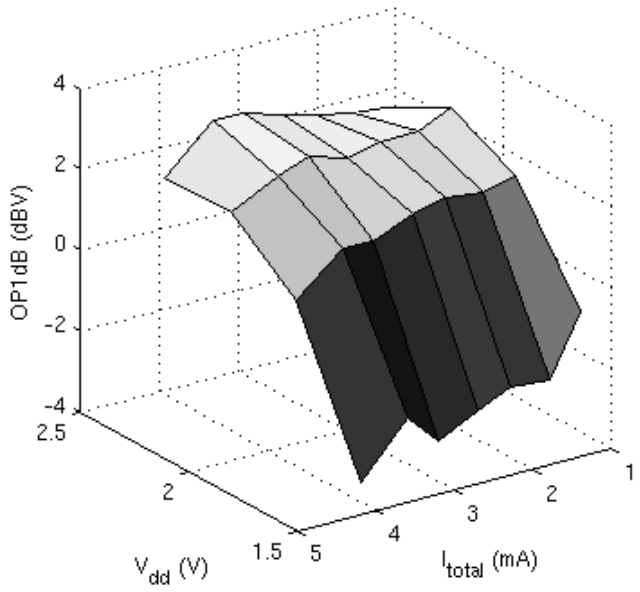


Figure 3.20: Simulated OP1dB of the common-gate input down-converter

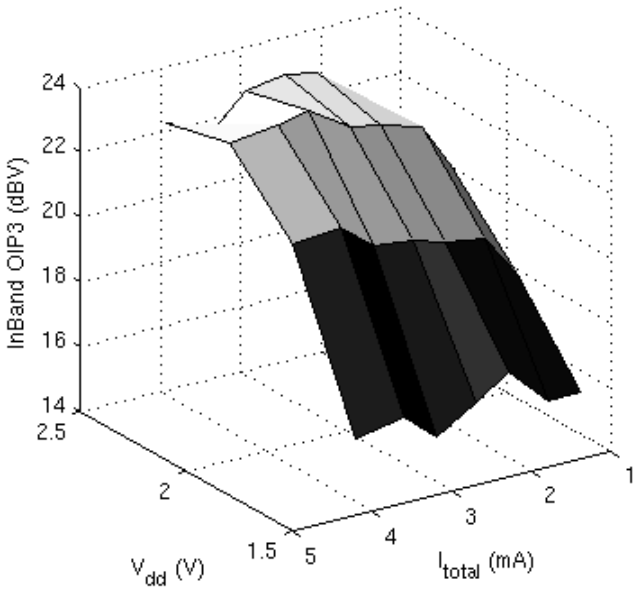


Figure 3.21: Simulated OIP3 of the common-gate input down-converter

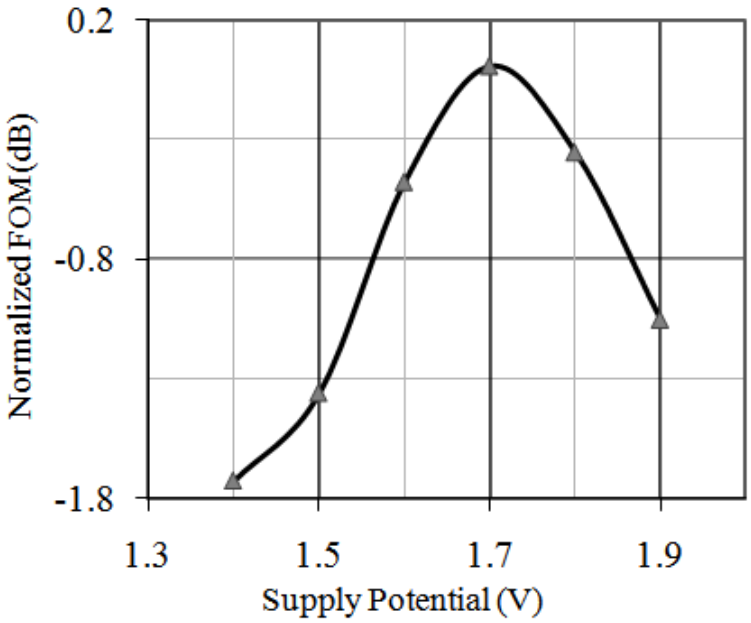


Figure 3.22: Normalized FOM for the common-gate input down-converter

3.6 Conclusion

A down-converter architecture incorporating a passive current mode mixer which re-uses the bias current between the RF transconductor and the baseband transimpedance amplifier in order to minimize power dissipation has been described in this chapter. The topology allows for current-sharing, while merging the operating voltage domains of the RF and baseband stages, that is, without the requiring an explicit intermediate local ground between the stacked RF and baseband stages. This feature is expected to make the design suitable for low-voltage applications. Low-frequency noise of the input transconductor has been suppressed using an active noise suppression technique. A circuit technique based on gain expansion is also demonstrated for

improving the IM3 performance with low power overhead. This technique employs controllable non-linear feedback in the transimpedance stage. Two different versions of this topology, one with a common-source and other with a common-gate input stage, are implemented. The CG version provides broadband input match. The CS implementation achieves a higher voltage gain and better sensitivity while trading off linearity (input-referred) performance. It is anticipated that the down-converter design will find application in systems where low-power requirement is critical, such as those for sensor networks, or for ISM band systems. Given the high FOM of the design, with suitable optimization, it can be anticipated that the topology can also find application in systems with greater dynamic range requirement such as cellular front-ends.

Table 3.2: Performance Comparison with Other Reported Mixers

	Frequency (GHz)	Vdd (V)	NF (dB)	Gain (dB)	IIP3 (dBm)	Power (mW)	Technology
CG input	1.0	1.8	9.8*	35	-9.2	4	180 nm CMOS
CS input	0.9	1.8	3.9*	46	-16.6	3.4	180 nm CMOS
[14]	2.0	1.5	3.1*	30	-12	12†	130 nm CMOS
[15]	2.4	0.6	11.8	12.7	-6.0	0.38	90 nm CMOS
[7]	2.4	1.8	12.9	15.7	1	8.1	180 nm CMOS
[26]	0.9	0.5	9*	12	-14	3.2†	180 nm CMOS
[27]	0.9	1.2	8.6*	29	-17.2	2.2	350 nm CMOS

*DSBNF was reported.

†Receiver with quadrature mixer was reported.

Chapter 4

A Power-Efficient Direct Conversion Receiver

4.1 Introduction

In this chapter, the design of a low power quadrature direct-conversion receiver (Fig. 4.1) and measurement results from its implementation are presented.

Each RF path of the receiver, consists of the common source input version of the down-converter described in Chapter 3. The input matching network is shared between the two RF signal paths which are driven by quadrature LO signals. An on-chip CML divider, shown in Fig. 4.2, is used for quadrature LO synthesis. The divider outputs were buffered and multiplexed with quadrature signals which could be potentially generated using off-chip source and phase shifting network in debug mode. The receiver includes techniques for achieving variable gain and reducing low frequency noise from the baseband stage, which are described below.

4.2 Variable Gain

The signal source drives the receiver differentially. The input is impedance matched using a π-section that is implemented on the board (Fig. 4.3). We

describe the in-phase (I)-path of the receiver below. The operation of the Q-path is identical.

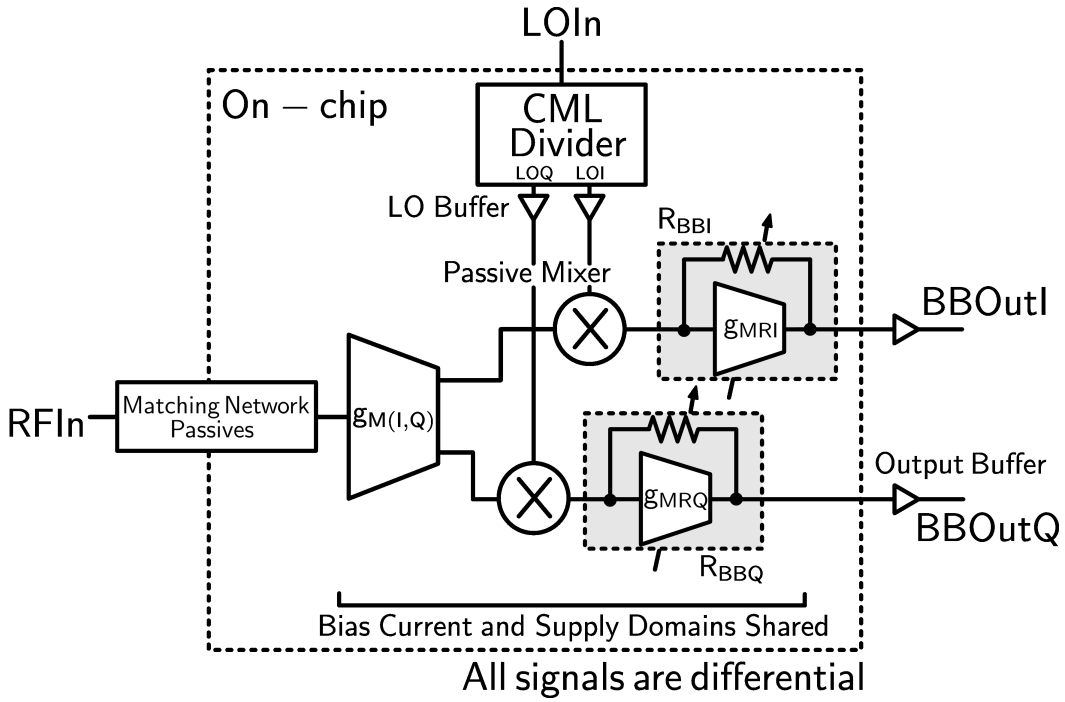


Figure 4.1: Block diagram of the receiver

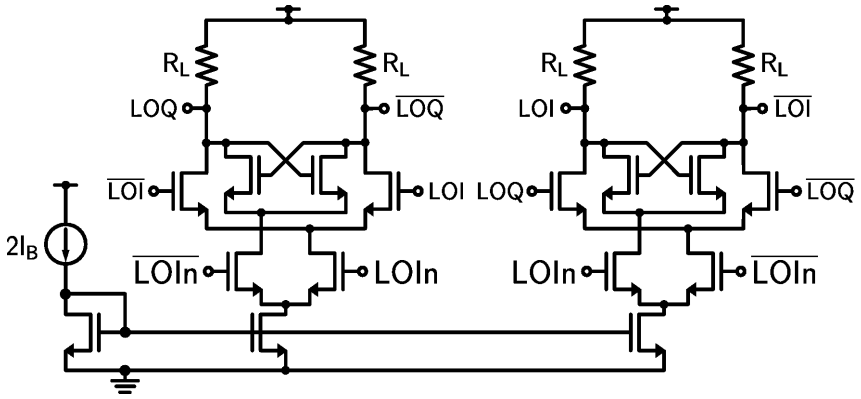


Figure 4.2: CML divider in LO path

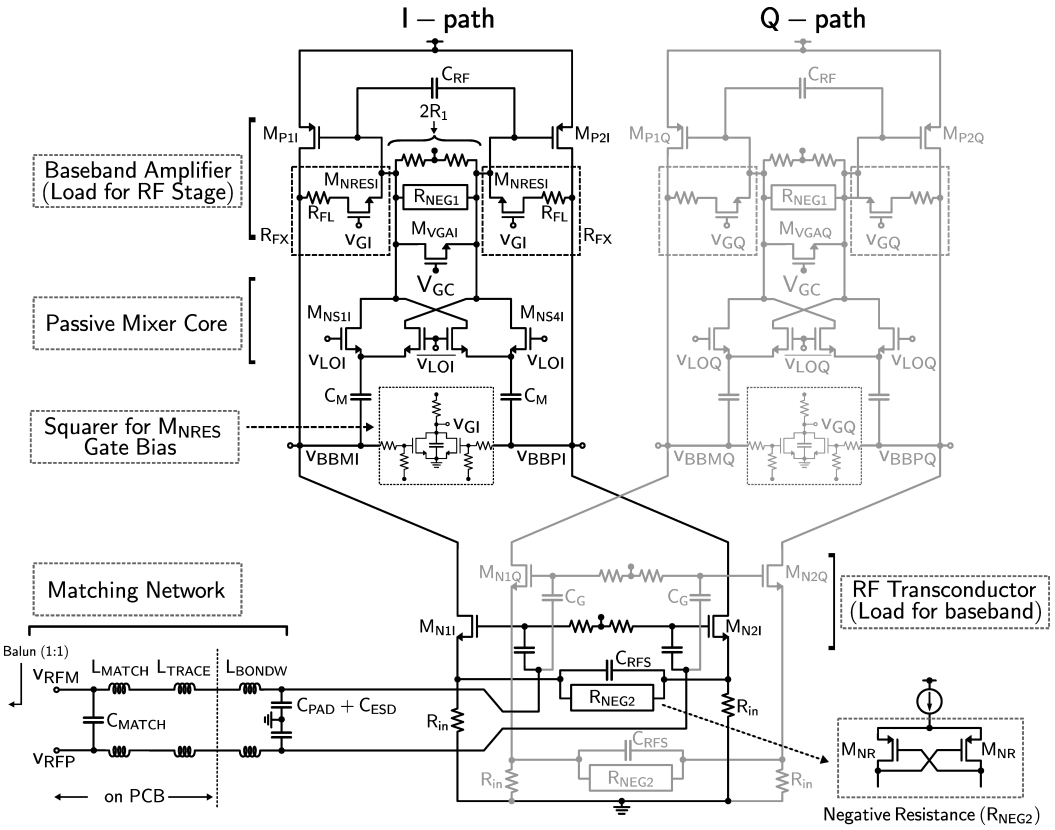


Figure 4.3: Receiver signal path (I-path in bold)

The RF voltage signal is converted into current (i_{RF}) by the input differential transconductor that is implemented using resistively degenerated NMOS devices M_{N1I} and M_{N2I}. The differential impedance looking into the devices M_{P1I} and M_{P2I} is of the order of $2R_{FX}$ and is thus high. On the other hand, the frequency translated impedance at the input of the mixer switching core is of the order of [1] $(8/\pi^2)(1/g_{mp})$ and is relatively much lower. Thus i_{RF}

[1]This is valid for the case when the gain of the receiver is at its maximum. When the VGA device, described later is ON, the resistance is further reduced due to the on-state resistance of the linear-mode MOSFET used for achieving gain variation.

flows into the passive mixer which is implemented here using NMOS switches M_{NS1-4I}. The switches commutate i_{RF} to provide a baseband current i_{BB}. A part of i_{BB} flows into the resistor formed by the NMOS device M_{VGAI}. Variation of R_{MVGAI} using the gate control voltage V_{GC} changes i_{MVGAI}. The remainder of the downconverted current ($i_{BB} - i_{MVGAI}$) flows predominantly into the feedback resistor R_{FX} and is termed i_{RFX}. This allows for VGA functionality.

The current i_{RFX} is converted into voltage at the drains of M_{P1I} and M_{P2I} through R_{FX}. The baseband signals are prevented from re-entering the mixer by C_M and are observed off-chip using unity-gain PMOS buffers, which isolate the drain nodes of the RF devices from the external load.

4.3 Baseband Noise Suppression

The $1/f$ noise of M_{P1I} and M_{P2I} degrades sensitivity. As mentioned in the previous chapter, looking back into the baseband outputs of the passive mixer switches, we see an effective differential resistance $2R_1$ (Fig. 4.3), which is primarily determined by a switched capacitor resistance $\propto 1/(f_{LO}C_{par})$, where C_{par} is the parasitic capacitance at the drains of M_{N1I} and M_{N2I}.

This impedance has a significant impact on the total output noise of the receiver. Specifically, the drain flicker noise current of M_{P1I} and M_{P2I}, $\overline{i^2_{dn,1/f}}$, appears as a noise voltage $\sim \{(R_{FL}+R_1)/(1+g_{mp}R_1)\}^2\overline{i^2_{dn,1/f}}$ V^2/Hz at the drains. To reduce $\overline{i^2_{dn,1/f}}$, the widths and proportionally the lengths of M_{P1I} and M_{P2I} can be increased. This increases the device area. However,

this also increases C_{par}, which degrades the conversion gain by increasing the attenuation of RF current at the drains of the NMOS devices. This also degrades the thermal noise limited sensitivity. R_1 which is proportional to $1/(f_{LO}C_{par})$, also decreases, which in turn limits the improvement in $1/f$ noise voltage. Conversely, if the widths of M_{P1I} and M_{P2I} are reduced to decrease C_{par}, then $\overline{i^2_{dn,1/f}}$ itself increases, which increases the noise voltage caused by $1/f$ noise sources.

To avoid this trade-off, a cross-coupled PMOS pair M_{NR} ("R_{NEG1}" in Fig. 4.3) is used at the PMOS gates, which increases the value of R_1. This reduces the $1/f$ noise and also allows for using smaller sized M_{P1I} and M_{P2I} which lowers C_{par} and in turn improves conversion gain. The principle of operation is captured in the Fig. 4.4. In the implementation the transconductances of the devices M_{NR} constituting R_{NEG1} were chosen to optimize the flicker noise corner under maximum gain condition in the nominal process. A similar technique is reported in [28] for a passive downconverter with separate

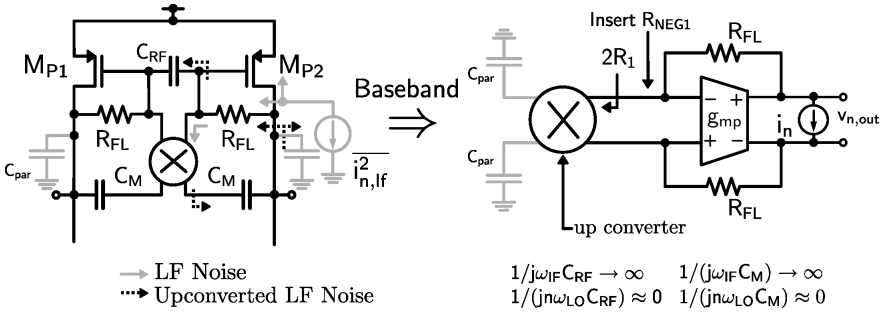


Figure 4.4: Conceptual illustration of suppression of flicker noise from baseband transconductors

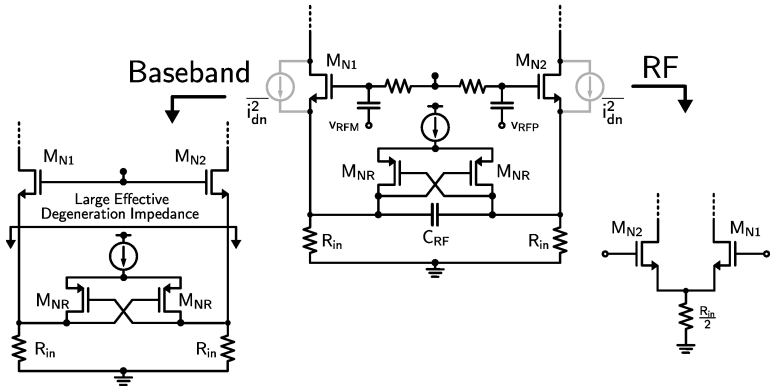


Figure 4.5: Network for suppression of flicker noise from RF transconductors

bias current legs for RF and baseband [12].

The baseband noise from the devices M_{N1I} and M_{N2I} is suppressed with a negative resistance (R_{NEG2}) in shunt with R_{in} as discussed in Chapter 3. The frequency dependent transformation of the source network is shown in Fig. 4.5. It is noted that this is similar in operation to the use of R_{NEG1}, since in both cases, the effectiveness of the baseband feedback networks is increased by using a negative resistance.

The signal voltages across R_{NEG1} and R_{NEG2} are small, and thus they have no measurable impact on linearity. R_{NEG1} and R_{NEG2} use large PMOS devices with small current (~200 μA) for minimizing their $1/f$ noise. It should be noted that R_{NEG1} and R_{NEG2} are both connected across nodes where the shunt positive resistance is much lower than negative resistance contributed by these cross-coupled devices. As such these active negative resistors cannot lead to instability. For example, the net resistance at the source nodes of M_{N1} and M_{N2} is set primarily by the transconductance of these devices,

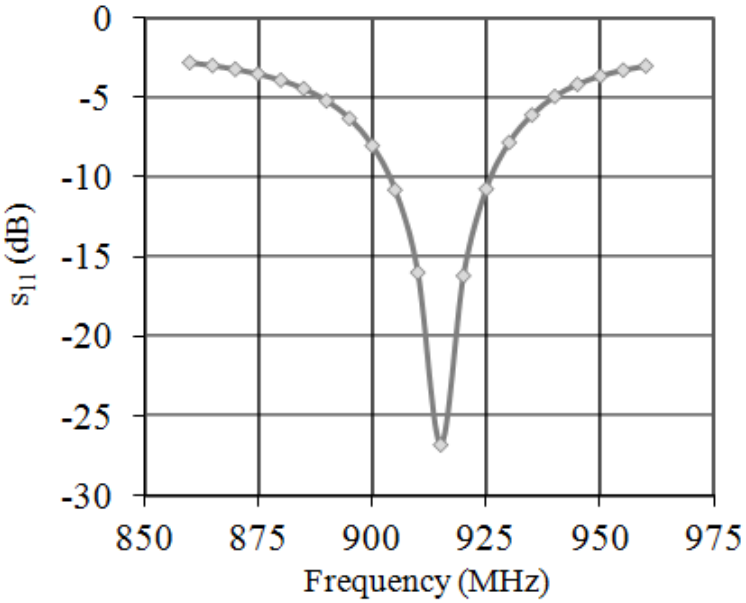


Figure 4.6: Measured input reflection coefficient

which is significantly smaller that the magnitude of R_{NEG2} as determined by the size of the resistance R_{in}. Similarly, at the gate nodes of M_{P1} and M_{P2} the impedance is set by their transconductances, due to resistive shunt-shunt feedback, being significantly small compared to magnitude of R_{NEG1} which is set by the impedance looking back into the passive mixer.

4.4 Measurement Results

The receiver was implemented in a 0.18-μm CMOS process. The ICs were housed in 48 pin TQFP packages and measured on-board. The conversion gain from 905 MHz – 925 MHz was 44.5±1 dB with $|s_{11}|$ lower than -10 dB (Fig. 4.6). The gain could be varied by up to 18 dB (Fig. 4.7).

The native IF-bandwidth of the receiver was greater than 10 MHz. However, due to the capacitance of PCB traces and output impedance of on-chip buffer the bandwidth was limited to 6 MHz as shown in the inset of Fig. 4.7. An optional external capacitor (C_{FILT}) was used in parallel with the on-chip C_{RF} for ease of testing and control of the receiver bandwidth. The resistance looking into the PMOS ($M_{P(1,2)}$) gates allowed for bandwidth of the order of MHz with total capacitance of the order of several tens of pF, which can be integrated if required without significant area penalty. Further filtering can be implemented using a capacitor partially shunting R_{FL}. However, this was not implemented.

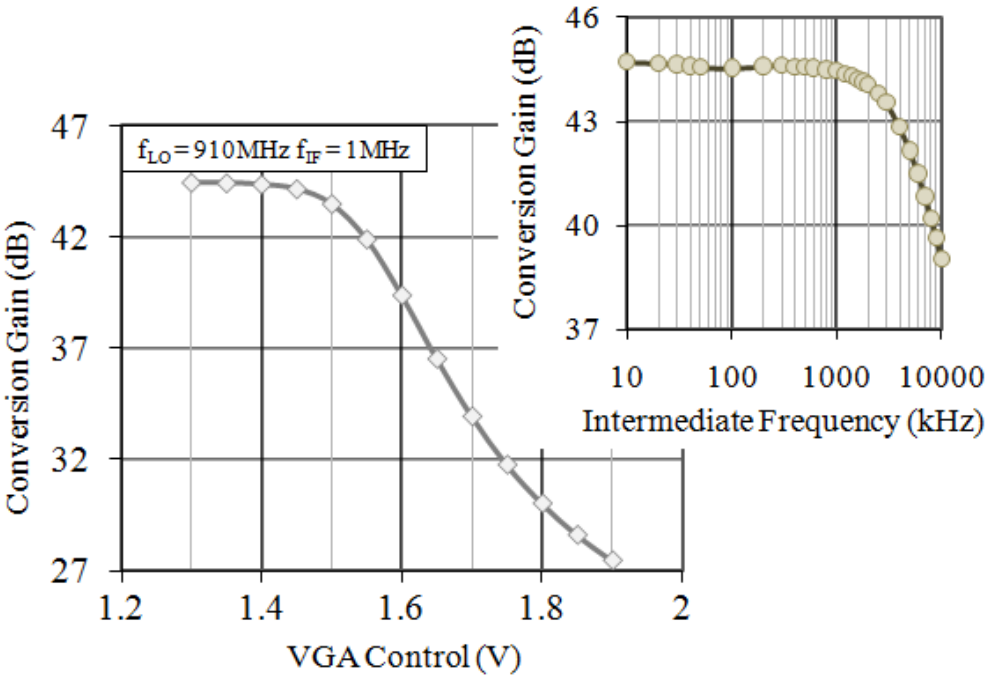


Figure 4.7: Measured gain control curve

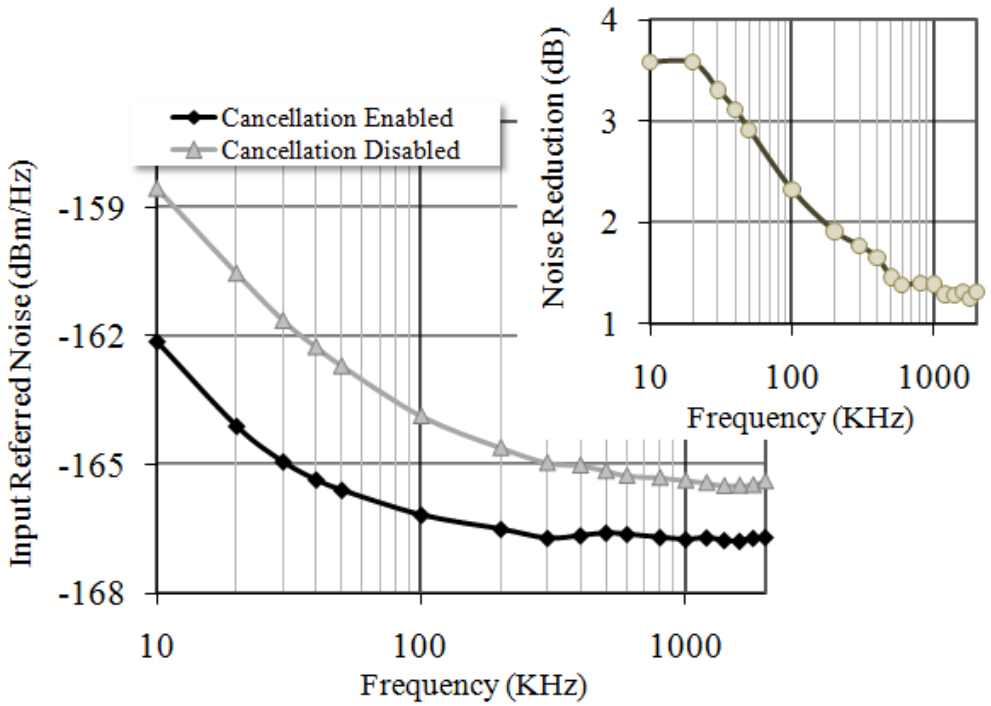


Figure 4.8: Receiver input referred noise with noise cancellation circuits turned ON or OFF

With the baseband noise suppression circuits enabled, the low frequency noise decreased by about 3.5 dB at 10 kHz (Fig. 4.8) while the flicker noise corner frequency reduced from 43 kHz to 18 kHz. The DSBNF at 1 MHz IF was 4.3 dB.

The in-band IIP3 (using tones at offset 1.3 MHz and 1.7 MHz from the LO), was -14.5dBm (Fig. 4.9). The output IM3 improved by approximately 18 dB with non-linearity cancellation. The in-channel P1dB was 0 dBVp at the output for peak gain, and was set by output swing limit. The blocker 1-dB compression with a 5 MHz offset interferer was seen to improve by 5 dB for

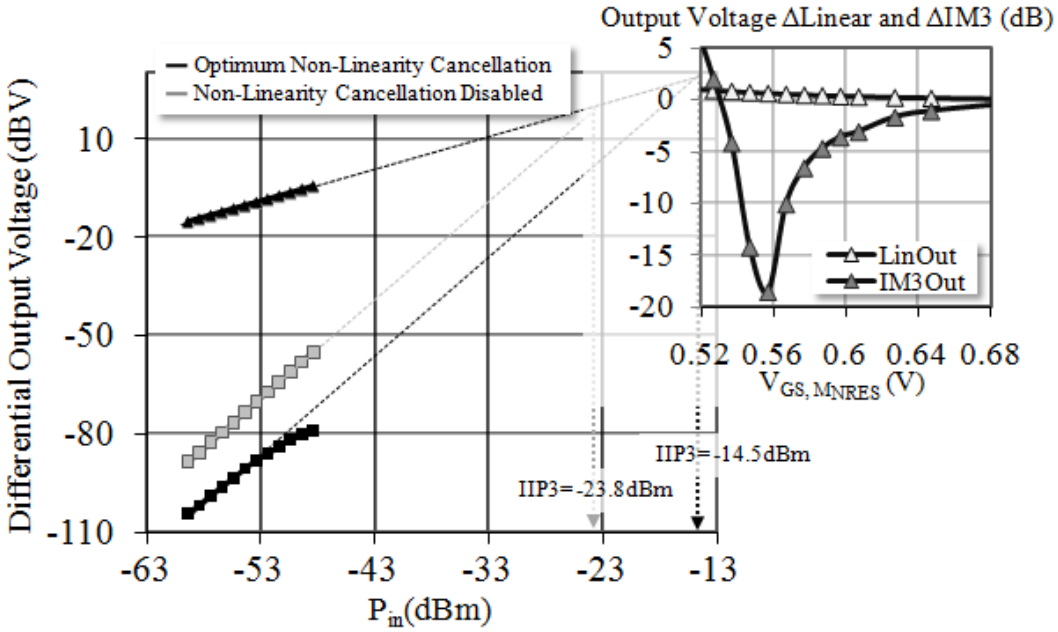


Figure 4.9: Receiver in-band IIP3 with and without non-linearity cancellation

C_{FILT} setting corresponding to 2 MHz baseband bandwidth.

The variation of DSBNF and output compression point as a function of the conversion gain is captured in the Fig. 4.11 and Fig. 4.12. It is seen, as expected, there is a tradeoff between noise and linearity as the gain is decreased from the peak value.

The design achieved amongst the highest reported receiver dynamic range FOM [15] of 26.7dB without requiring integrated inductors. The total area requirement was 0.5mm^2 including the LO circuits (Fig. 4.13). The PCB used for mounting and measurement is shown in Fig. 4.14. The summary of the measured performance is given in Table 4.1 and it is compared against other receiver implementations in Table 4.2.

Table 4.1: Measured Performance Summary

Metric	Value
Max Conversion Gain at 0.91 GHz	44.5 dB
VGA Range	18 dB
$\|S_{11}\|$	$\leq$ -10 dB over 20 MHz BW
DSBNF at 1 MHz IF	4.3 dB
Flicker Noise Corner	18 kHz
Output P_{-1dB}	0 dBV
Inband OIP3	20 dBV
Inband IIP3	-14.5 dBm
IIP2 (Uncalibrated)	25 dBm
Current (I+Q)	2 $\times$ 2.2 mA
Supply Voltage	1.8 V
Technology	0.18-μm CMOS
Area	0.5 mm^2

Table 4.2: Receiver Performance Comparison

	Frequency (GHz)	Vdd (V)	NF (dB)	Gain (dB)	IIP3 (dBm)	Power† (mW)	CMOS Tech§	FOM* (dB)
This Work	0.91	1.8	4.3	44.5	-14.5	4	180 nm	26.7
[29]	2.40	1.8	7.3	30	-8	3.1	180 nm	23.7
[30]	0.91	1.2	8	-	-22	1.3	130 nm	-
[31]	0.88	1.5	1.7	33	-9.9	11	65 nm	24.5
[32]	2.35	1.2	24.5	52	-21‡	2.5	130 nm	13.6
[33]	2.40	1.8	4.4	25.7	-6.5	4.4	180 nm	23.7
[11]	1.6	1.2	4.8	36	-19	4.2	130 nm	24.4
[34]	0.9	2.7	3.8	-	-20	21	SiGe BiCMOS	-

†Receiver with quadrature mixer was reported. FOM uses 0.5 x PowerLNA + PowerMixer_BB I or Q

*NF metric used in FOM is DSBNF + 3 dB where applicable.

‡100 Ohm input impedance.

§unless stated otherwise.

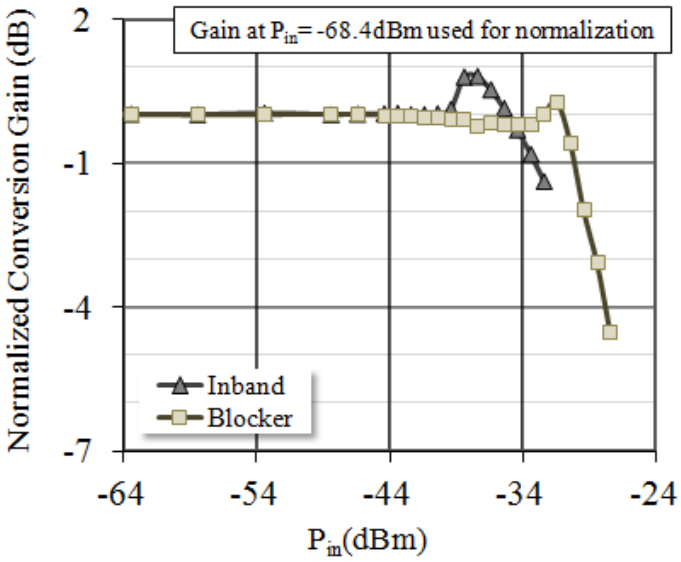


Figure 4.10: Receiver gain compression curves

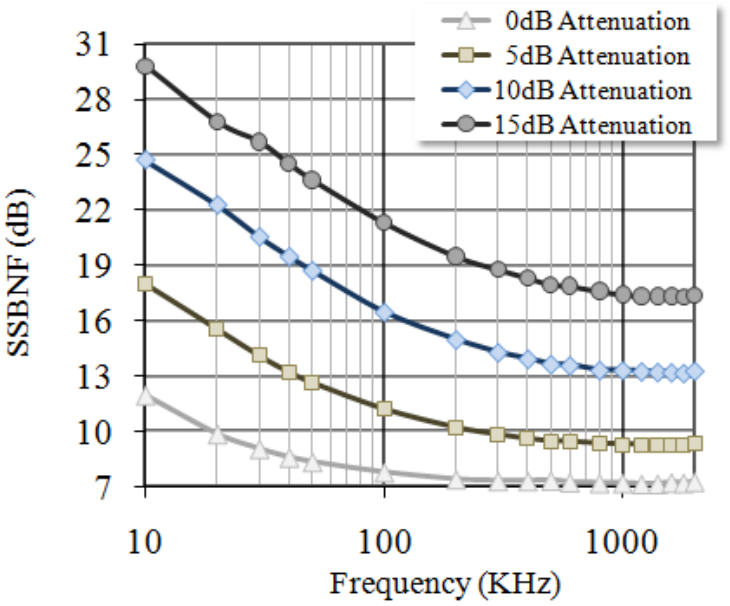


Figure 4.11: Measured noise figure variation with VGA setting

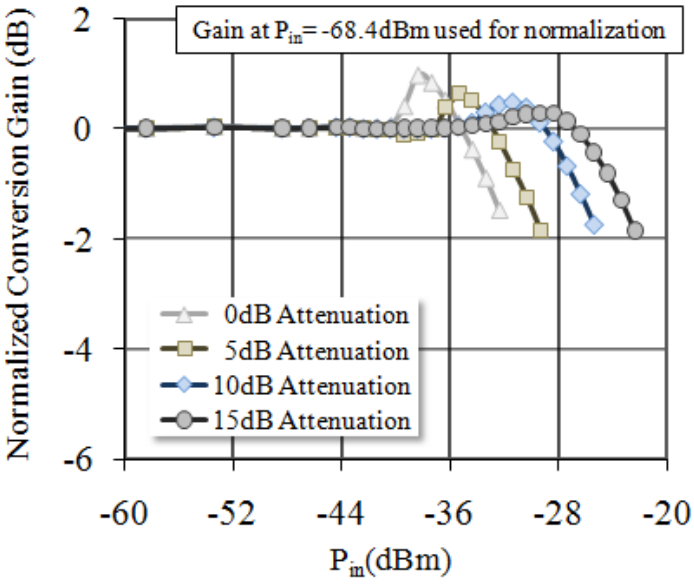


Figure 4.12: Measured compression point variation with VGA setting

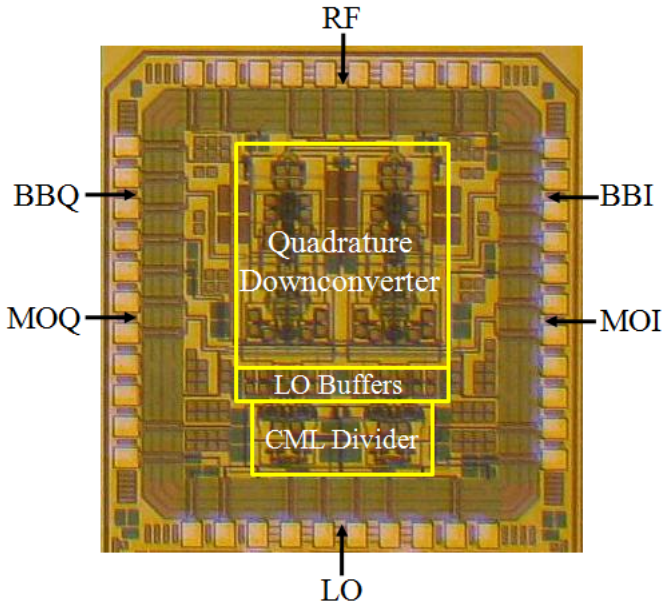


Figure 4.13: Die photograph

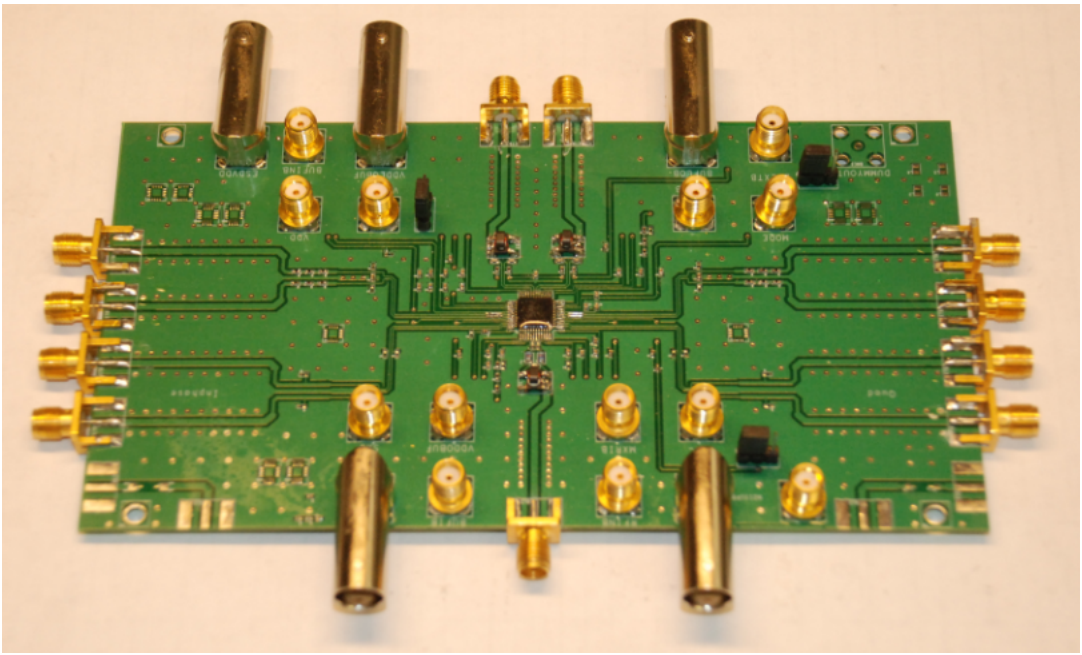


Figure 4.14: Printed circuit board used for receiver measurement

Chapter 5

Power-Efficient Oscillator Topologies

5.1 Introduction

Oscillators are key building blocks in communication systems, as they are used to provide a time or frequency reference. In radio-frequency transceivers these circuits are typically used as part of the frequency synthesizer. These circuits are autonomous, in that they utilize their intrinsic device noise in combination with a frequency selective network for operation. The reliance on device noise however, leads to a fundamental performance limitation, i.e., the one-sided output power spectrum of an oscillator which should ideally be an impulse function at the frequency of interest with a well-defined amplitude, is not so. The output of the oscillator is instead usually characterized by a shaped power spectral density, that is localized in frequency [35]. In this chapter we will briefly review this non-ideality and other key performance metrics of oscillators. We will conclude with a survey of prior work on oscillator topologies that are optimized for power efficiency.

5.1.1 Oscillator Specifications

The practical oscillator output can be approximated by

$$v_{osc}(t) \quad = \quad V_{osc}(1 + a(t))f(\omega_{osc}t + \phi(t)) \tag{5.1}$$

where $\phi(t)$ and $a(t)$ are functions of time, f is a periodic function representing the shape of the steady-state output waveform of the oscillator [36]. Due to the fluctuations represented by $\phi(t)$ and $a(t)$, the spectrum of the oscillator has sidebands close to the frequency of oscillation ω_{osc} and its harmonics[1]. Such short term instability of an oscillator is characterized using the single sideband noise spectral density. It is defined as,

$$\mathcal{L}_{total}\{\Delta\omega\} \quad = \quad 10\log_{10}\frac{P_{sideband}(\omega_{osc} + \Delta\omega, 1\,\text{Hz})}{P_{carrier}} \tag{5.2}$$

where $P_{sideband}(\omega_{osc} + \Delta\omega, 1\,\text{Hz})$ represents the single sideband power at a frequency offset $\Delta\omega$ from the carrier, in a measurement bandwidth of 1 Hz. $P_{carrier}$ is the total power in the spectrum. Although $\mathcal{L}_{total}\{\Delta\omega\}$ includes the components due to amplitude and phase fluctuations, in practical oscillators due to amplitude limiting, it is dominated by the phase portion $\mathcal{L}_{phase}\{\Delta\omega\}$ [36]. Additionally, in transceiver applications, very frequently the mixers employed use amplitude limiting on the LO port, in which case too, amplitude noise is not of significance.

[1] In a strict sense, for a noise driven oscillator, it is not possible to see a unique oscillation frequency [37].

Oscillator phase noise is a significant source of performance degradation in communication transceivers. In receivers, phase noise degrades the noise performance due to reciprocal mixing with blockers (Fig. 5.1). Phase noise minimization is critical for ensuring high sensitivity in frequency bands where large blockers [38] are present and not sufficiently attenuated by preselect filters. Oscillator phase noise also impacts the Error Vector Magnitude (EVM) in several modulation schemes. Low noise oscillators are also required in precise time references for many mixed-signal systems, such as continuous time $\Sigma\Delta$ ADCs.

Apart from phase noise, another key oscillator metric is its tuning range (f_{TR}). To accommodate the frequency span required by any specific standard and also to combat the process variation induced drift, the oscillation frequency needs to be tunable about a nominally expected value. Typically this is achieved by varying passive elements which determine the oscillation time constant, e.g., using switched capacitors and varactors, or through changing bias currents. If this tuning is controlled by an external voltage, the circuit its termed a voltage controlled oscillator (VCO).

Apart from phase noise and tuning range, linearity of the VCO tuning curves with respect to the control voltage and area required are its important metrics.

Both phase noise and tuning range are tied to the power requirement imposed by the oscillator whose power efficiency is typically represented by a metric that is inversely proportional to the product of phase noise and power

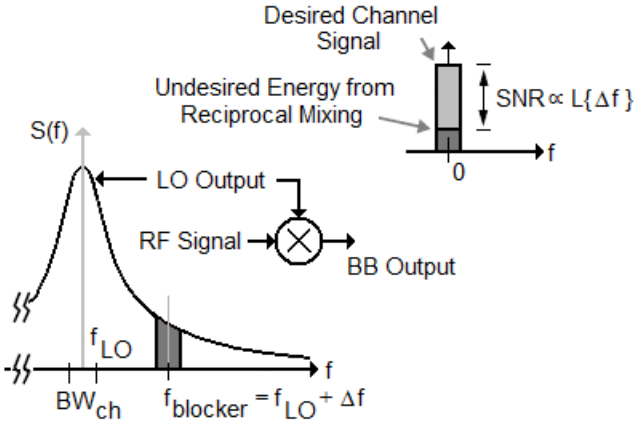


Figure 5.1: Reciprocal mixing in direct conversion receivers

and directly proportional to the fractional tuning range given by $100 \times f_{TR}/f_{osc}$. In the following subsection we survey several design techniques for the purpose of minimizing the product of phase noise and power in order to enhance the oscillator power efficiency.

5.1.2 Prior Work on Power-Efficient VCOs

A large number of techniques have been investigated for minimizing the phase noise or maximizing the power efficiency of the oscillators. Of the three types of oscillators implemented in ICs, namely, ring, relaxation, tuned LC oscillators, the LC tank based designs provide the best phase noise at a fixed power. This is due to the high quality factor of the resonant tanks. The power dissipated per cycle, as a fraction of the energy stored in the resonator is small in such designs, compared to the non-resonant approaches. The resonator based approach is thus seen to dominate in wireless transceiver

applications. Some of the prior optimization techniques for LC oscillators are briefly reviewed below.

Fig. 5.2(a) shows a phase noise optimized cross-coupled LC oscillator topology proposed in [39] where passives C_{filt} and L_{ser} are used to reduce phase noise with ideally no power penalty. C_{filt} is used to filter the bias noise generated around the second harmonic of the oscillation frequency (ω_{osc}) which can contribute to phase noise after being commutated by the cross-coupled pair. L_{ser} is used to resonate any parasitic capacitance (C_{par}) at the common-source node of the cross-coupled pair at the second harmonic of the oscillation frequency ($2\omega_{osc}$). This reduces the periodic loading of the tank caused by the active device going into triode region around time instants of peak swing. The consequent increase in effective tank quality factor improves noise performance.

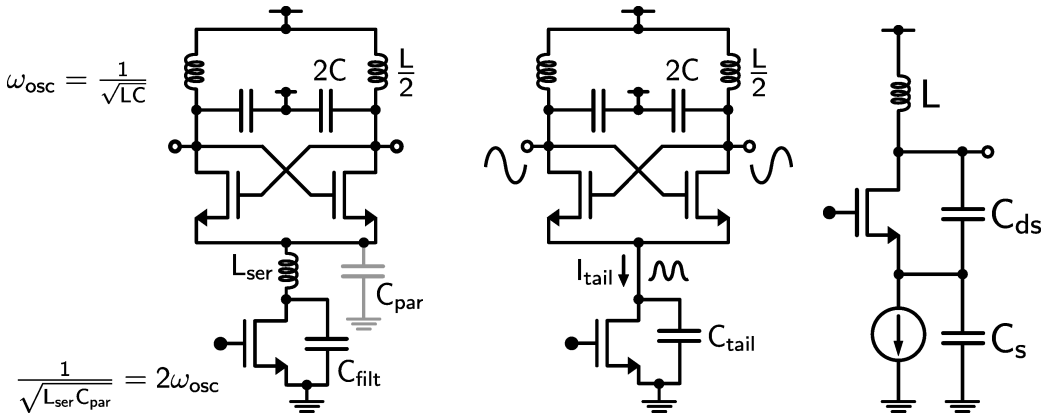


Figure 5.2: LC Oscillator (a) With noise filter (b) With tail current shaping (Class-C) (c) Colpitts oscillator

Another optimization technique was proposed in [40] and [41]. This design uses a capacitor C_{tail} as shown in Fig. 5.2(b) to increase the amplitude of oscillation by synthesizing an effective tail current which is a superposition of a DC and a current at frequency $2\omega_{osc}$. The DC is upconverted while the current component at $2\omega_{osc}$ is down-converted to the fundamental frequency. Both components add to the oscillation amplitude. The authors in [41], however, point out that the optimization works only for swings which do not force the cross-coupled pair devices into the triode region. In this topology, the cross-coupled pair periodically provides a energy replenishing current (I_{tail}) to the tank to compensate for the tank losses. A different interpretation of the noise reduction mechanism is based on the observation that the maxima of the current I_{tail} are synchronized with the peaks of output swing. As such, the maximum noise from the cross-coupled devices is also observed at the peak swing. Since these are also the instants when the phase is least sensitive to perturbations, the resulting phase noise is minimized. The cross-coupled pair in this topology is stated to be operating in class-C mode [41] since ideally, at zero-crossing of the output, none of the cross-coupled device conduct any current. The phase noise improvement resulting from such waveform shaping can be explained rigorously using impulse sensitivity function (ISF) based analysis as proposed by [36].

A widely used low phase noise topology is the Colpitts oscillator (Fig. 5.2(c)). In this design, the noise current is minimized at the time points where the voltage goes through its zero-crossing. Since the phase of the output is

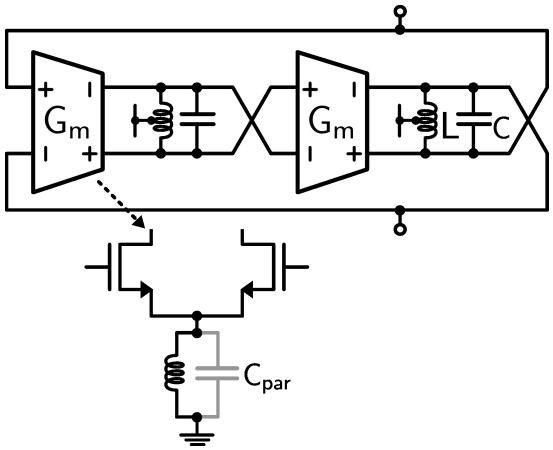


Figure 5.3: Cascaded LC ring oscillator

most sensitive to noise injected at the zero crossing, the design inherently can offer a low phase noise for a given power dissipation. An optimized differential version of the Colpitts oscillator was proposed in [42] .

VCOs that employ multiple cores for the purpose of reducing phase noise, have also been demonstrated in literature, e.g. [43], [44]. [43] employs multiple cascaded LC stages in a global feedback loop, which satisfies the Barkhausen criterion for oscillation. A two-stage version is shown in Fig. 5.3. It is shown in [43] that by appropriately power combining the outputs of the cores by using transformers, the phase noise can be improved linearly at the expense of power, over a wide bandwidth. A different implementation using a transformer based pickup loop spanning across multiple oscillator cores is demonstrated in [44].

Complementary oscillator cores have been shown to potentially achieve low phase noise. The theoretical bound on phase noise performance of such

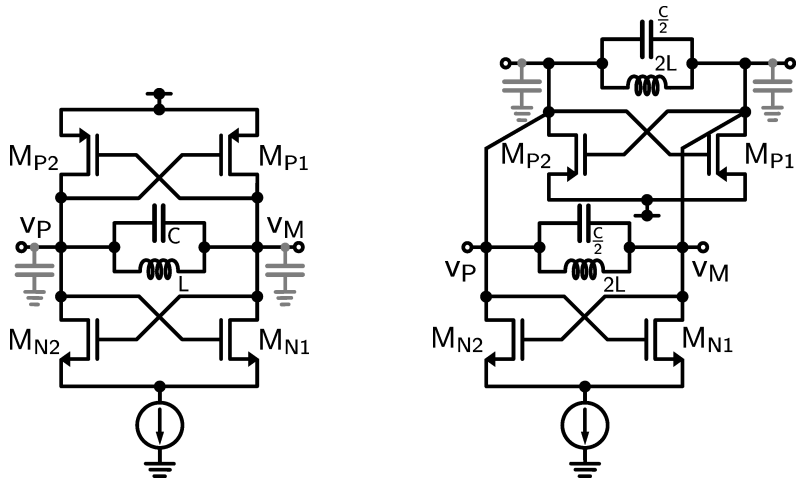
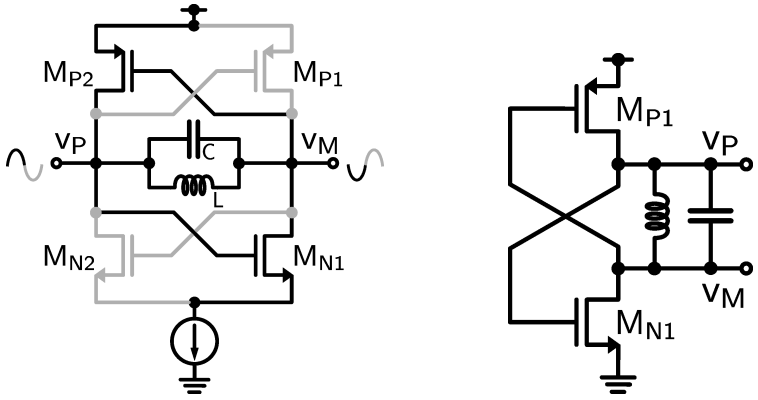


Figure 5.4: LC oscillator (a) CMOS (b) Direct coupled NMOS and PMOS oscillators

an oscillator is discussed in [45] along with a comparison to an NMOS-only oscillator. Such an oscillator (Fig. 5.4(a)) can be thought of as implementing current-reuse between two separate oscillator cores, one NMOS and other PMOS, which are direct-coupled (Fig. 5.4(b)). As will be explained in next chapter such coupling ideally should lead to 3-dB phase noise improvement assuming that the bias current generator is noiseless and the complementary devices contribute similar amount of noise. However, due to the asymmetry in the structure arising from the absence of a high impedance current sink associated with the PMOS core, this improvement is not practically achieved for large swing.

A variant of the complementary oscillator has been proposed in [46] (Fig. 5.5(b)). It can be thought of as a half-circuit version which allows current



(a) (b)

Figure 5.5: LC oscillator (a) CMOS (half-cycle in bold) (b) CMOS half-circuit

flow through the tank every half-cycle. To reduce headroom requirement the design does not include any bias current source. However, the design is not symmetric with respect to the differential output nodes.

Chapter 6

A VCO Employing Current Reuse and Capacitive Power Combining

6.1 Introduction

In the last chapter we reviewed several previously reported design techniques for minimizing phase noise in LC oscillators (Fig. 6.1(a)), e.g. bias current noise filtering using passive networks [39], modulating current in switching pairs [40] and coupled multi-stage oscillators [43]. In general, for any oscillator topology, lowering of phase noise under a DC power constraint imposes a significant design challenge.

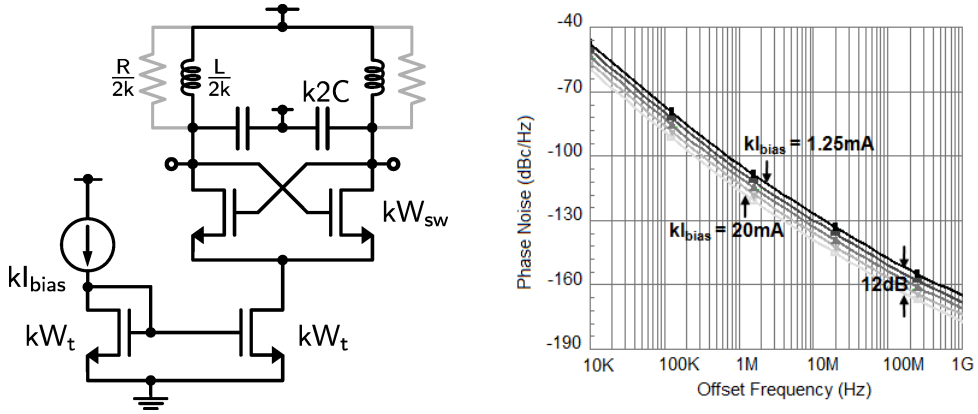
In this work we demonstrate a technique to combine AC power from multiple oscillator cores to minimize phase noise while simultaneously constraining DC power through current reuse among the cores. This improves the power efficiency of the design over conventional implementations. The reported technique also mitigates modeling uncertainty that can arise from simultaneous impedance scaling in the oscillator tank and current scaling in the cross-coupled core, as described below. The primary goal of this design is to minimize distant phase noise with adequate power efficiency, while not degrading close-in phase noise. This is critically important in platforms where

multiple radios in close proximity operate simultaneously in the same band, such as Bluetooth, WiFi and WiMax (2.4-2.5 GHz). Additionally, when using a low noise oscillator in combination with a high-linearity receiver, the pre-select filter can be simplified or eliminated, thereby reducing cost and lowering insertion loss.

6.2 Phase Noise Optimization

6.2.1 Capacitive Power Combining

In principle, one can improve phase noise performance by simultaneously increasing current and scaling down all impedance levels in a stand-alone oscillator. The phase noise is reduced because the output noise voltage is decreased while the oscillation amplitude is held constant. This can be inferred from [47]. It is to be noted that optimum phase noise performance is achieved



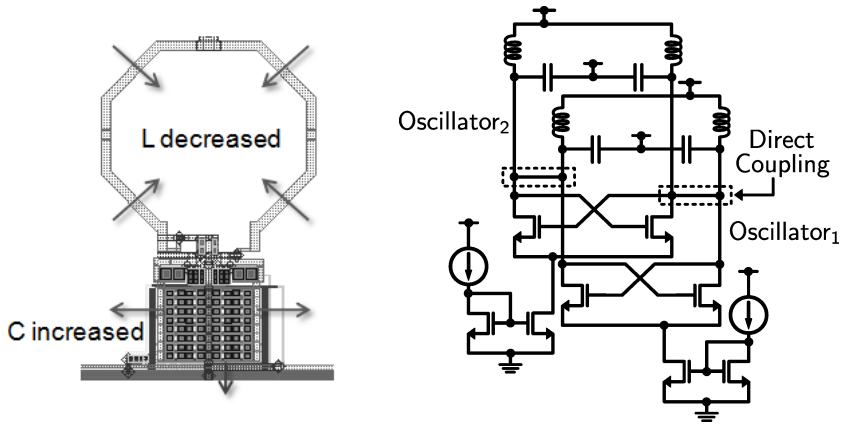
(a) (b)

Figure 6.1: Conventional LC oscillator (a) Impedance and bias current scaling (b) Impact of scaling on phase noise

for an operation at the boundary between the current and voltage limited regime [48]. Therefore for phase noise to be improved by increasing current it is necessary to scale down the impedance. Otherwise, the oscillator will enter the voltage limited regime thereby leading to potential degradation of phase noise. The simulated variation of phase noise in a conventional LC oscillator (Fig. 6.1(a)) under such idealized scaling is shown in Fig. 6.1(b).

However, scaling down impedances leads to modeling uncertainty due to inductive parasitics of large capacitors (C). A representative layout of a wide tuning range VCO (Fig. 6.2(a)) shows how such scaling leads to increased routing parasitics of switched capacitor array. Similarly, the uncertainty in estimation of the inductance also increases due to proximity of neighboring routings. Moreover, if the size of the inductor is decreased, the inductance (L) scales more rapidly than its series resistance[1], leading to degradation in Q, if the inductor is used at a constant frequency [49]. These impediments pose a practical limit on improving the phase noise performance that can be achieved by increasing current. To mitigate the issues arising from impedance scaling, we employ multiple spatially separated, but electrically connected [50] oscillators as shown in Fig. 6.2(b). This approach extends the range over which current can be traded linearly with a decrease in phase noise, without getting limited by the parasitics of scaled capacitors and inductors. Although Fig. 6.2(b) shows the degenerate case for such an oscillator, it serves as a basis

[1]For example, if the diameter of a single-turn inductor is decreased then the resistance decreases linearly while the inductance decreases super-linearly.



(a) (b)

Figure 6.2: Power combining (a) Physical impact of scaling passive impedances (b) Electrically coupled oscillators

for understanding the bias-current-shared oscillator topology to be discussed in the following section. Capacitive coupling is employed when connecting oscillators with nodes at different DC potentials.

Capacitive coupling is a technique for power combining in oscillators. In this approach, differential currents from multiple cross-coupled pairs that provide the required negative resistance are injected into a distributed resonant network. Transformer coupling provides an alternative for power combining. However, it is not used in our work due to layout constraints.

6.2.2 Mode Selection in Capacitively Power Combined Oscillators

In this section, we consider capacitive coupling of two conventional LC oscillators (Fig. 6.3(a)), and analyze the impact of this coupling on the dynamics of oscillation. We use the topology to demonstrate the operating

principle, which holds for different implementations of core oscillators, and also for a larger number of oscillators, N. Each of the two tanks is assumed to consist of a differential capacitor (C) and inductor (L). We assume single-ended lossless coupling capacitors (C_c) between the two oscillators. The output is observed at nodes located symmetrically between the two oscillator cores as shown in the figure.

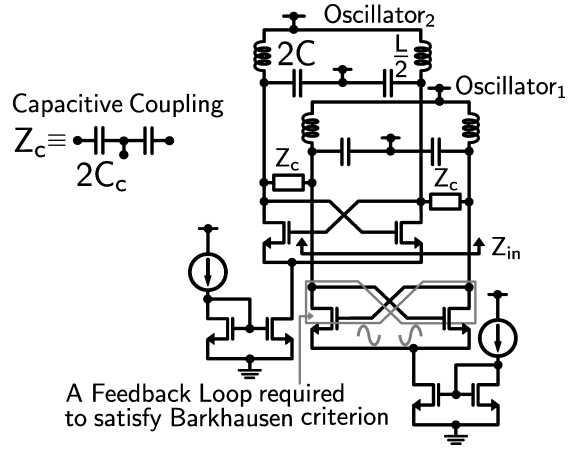
The use of a high (> 2) order coupled load results in the possibility of multiple frequencies of oscillation. We show here that through proper selection of design parameters, the desired steady state oscillation frequency can be achieved.

The Barkhausen criterion imposes a 360° phase shift requirement around the feedback loop (Fig. 6.3(a)) which is split equally between half circuits due to midline symmetry. This ensures that the individual cores have differential output voltages, and common-mode oscillation does not occur. Consequently, we can analyze the impact of the coupled load, looking differentially into it. We denote the coupled resonator load impedance looking differentially from the output of each core, *e.g.* Oscillator$_1$ in Fig. 6.3(a), as $Z_{in}(s)$. $Z_{in}(s)$ can be expressed as shown in (6.1) through (6.3).

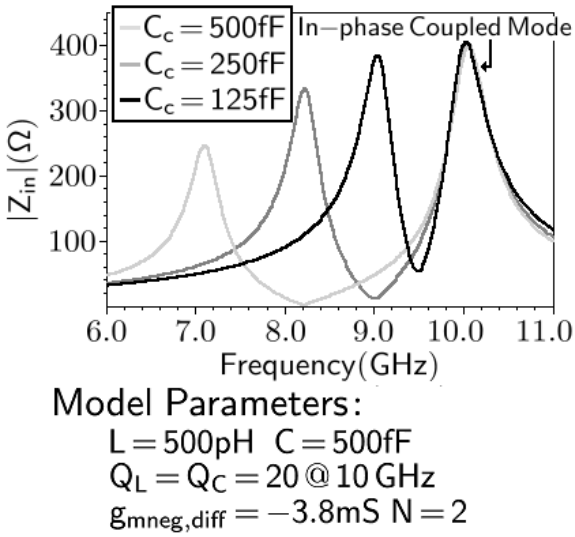
$$Z_{in}(s) = \frac{N(s)}{D(s)} \tag{6.1}$$

$$N(s) = sLR_1(s)(s^2L(C + \frac{C_c}{2})R_2(s) + sL + R_2(s)) \tag{6.2}$$

$$D(s) = (1 + s^2LC)(1 + s^2L(C + C_c))R_1(s)R_2(s) + sL(R_1(s) (1 + s^2L(C + \frac{C_c}{2})) + R_2(s)(1 + s^2L(C + \frac{C_c}{2}))) + s^2L^2 \tag{6.3}$$



(a)



(b)

Figure 6.3: Coupled conventional LC oscillator (a) Capacitive coupling (N=2) (b) Typical Z_{in} looking into capacitively coupled load

where $R_1(s)$ and $R_2(s)$ are the effective shunt resistances of the two cores. The feedback in complementary core, *e.g.,* Oscillator$_2$, is not broken for evaluating $Z_{in}(s)$. Thus $R_2(s)$ includes the impedance boost provided by active cross-coupled pair in Oscillator$_2$.

There exist two frequencies at which $Z_{in}(s)$ is real and also exhibits local maxima in magnitude (*e.g.,* Fig. 6.3(b)). We denote those $Z_{in}(s)$ values by R_{par}. Using the expression of $Z_{in}(s)$, these frequencies can be shown to be $f_{inph} \approx 1/(2\pi\sqrt{LC})$ and $f_{antiph} \approx 1/(2\pi\sqrt{L(C+C_c)})$. For these frequencies, f_{inph} and f_{antiph}, nearly in-phase and anti-phase voltages are established respectively at the single-ended coupled output nodes of the two LC tanks when excited by a sinusoidal current. Oscillation can grow at either of these frequencies if the loop gain exceeds unity at startup, at that frequency.

If the resistance R_{par} of the coupled resonator is dominated by inductor loss, and C_c is large, then the anti-phase mode of oscillation has a lower value of R_{par} (Fig. 6.3(b)). These conditions, which are satisified by our design, follow from the observation that in the antiphase mode, the coupling path capacitance reduces the oscillation frequency, and hence the Q of the inductor, which leads to a reduction in R_{par}. Similar to above two modes, analogous oscillation modes will be initiated at the complementary oscillator core, *i.e.*, the output of Oscillator$_2$, and will have frequencies that are identical to Oscillator$_1$. At each mode frequency, similar but complementary phase differences between coupled nodes *i.e.,* ε vs. $-\varepsilon$ or $\pi - \varepsilon$ vs. $-(\pi - \varepsilon)$, where $\varepsilon \approx 0$, are established. When such multiple oscillation modes can po-

tentially start-up, cross-compression mechanisms amongst competing modes ensure that the mode with larger R_{par} (*i.e.*, a larger loop gain) eventually reaches sustained oscillation. Such mechanisms will be explained analytically in the next chapter.

Due to symmetry of the coupled load, either of the two possible modes, or their superposition, with identical frequency $\approx 1/(2\pi\sqrt{LC})$ originating from the each of the cores, eventually operate exactly in-phase. The frequency converges to $1/(2\pi\sqrt{LC})$ with ideally no current, apart from noise, flowing through a capacitive coupling path. This can be proven by adding the current phasors at the outputs of each core under the constraint of amplitude-limited frequency-locked operation in the steady state. Physically, the condition is established when the time-averaged negative transconductance of each core equals the respective LC tank shunt resistance.

The above arguments can be extended iteratively for coupling among a larger number of oscillators. The mode which reaches steady state corresponds to the case where all the star-connected coupled nodes are in-phase. It is noted that even for $N > 2$, $Z_{in}(s)$ has the same order and frequencies where it is real (*i.e.,* purely resistive).

Although the input impedance of the buffer is ignored in our derivation for simplification, the principles stated are valid even when it is explicitly considered and the buffer impedance merely modifies the oscillation frequency.

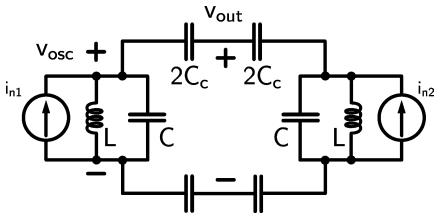


Figure 6.4: Far-out phase noise model for capacitively coupled conventional LC oscillator (N=2)

6.2.3 Far-out Phase Noise of Capacitively Power Combined Oscillators for In-phase Coupled Mode

In this section, we examine the impact of capacitive coupling on far-out phase noise performance. As above, we use the topology of two capacitively coupled conventional LC oscillators (Fig. 6.3(a)) to demonstrate the operating principle. We assume the oscillator has reached steady state and is operating in the in-phase coupled mode.

The noise model used for the analysis is shown in Fig. 6.4. As before, each of the two tanks is assumed to consist of a differential capacitor (C) and inductor (L). The effective parallel conductance ($1/R$) that models the losses of the LC resonators, and the negative conductance of cross-coupled transistors are not shown because for phase noise analysis we can assume that these terms exactly cancel each other [47]. A single-ended lossless capacitor (C_c) is used to couple the two oscillators.

The impedance of each resonator close to the oscillation frequency is given by

$$Z_r(\mathrm{j}\omega) = \frac{1}{\mathrm{j}2C\Delta\omega} \tag{6.4}$$

At frequency offsets which are large but still satisfy the constraint $\Delta\omega \ll \omega_{osc}$, the phase noise is dominated by the thermal noise from the active devices and resonators. The phase modulated (PM) components of currents (about LO sidebands) arising from these noise sources are denoted by i_{n1} and i_{n2}. These are injected into the lossless load and appear as oscillator phase noise. Each of the sources, i_{n1} and i_{n2}, sees an impedance of

$$Z_{cpl}(\mathrm{j}\omega) = Z_r(\mathrm{j}\omega) || \left[Z_r(\mathrm{j}\omega) + \frac{2}{\mathrm{j}\omega_{osc} C_c} \right] \tag{6.5}$$

The spectral density of i_{n1} is identical to that of i_{n2} and is given by

$$\frac{\overline{i_{n1}^2}}{\Delta f} = \frac{\overline{i_{n2}^2}}{\Delta f} = F \left[\frac{1}{2} \frac{\overline{i_{nR}^2}}{\Delta f} \right] \tag{6.6}$$

where the second factor is the PSD of the phase modulated current noise arising from R. The noise factor F, shown in equation (6.7), has been determined under the assumption of non-triode operation in [47] while considering the non-linear and time-varying nature of the system.

$$F = 1 + \frac{2\gamma I_{DC} R}{\pi V_a} + \frac{\gamma g_{mt} R}{4} \tag{6.7}$$

Here, I_{DC} is the current, V_a is the differential oscillation amplitude, γ is the excess noise factor and g_{mt} is the transconductance of the tail transistor for each coupled oscillator. It is noted that V_a and F for each core remains the same as for an uncoupled oscillator despite the change in the load impedance.

With uncorrelated noise contributions from the two sources, the far-out phase noise at the output is given by

$$2\frac{F}{2}\frac{\overline{i_{nR}^2}}{\Delta f}\left|Z_{cpl}(\mathrm{j}\omega)\right|^2\left[\frac{\omega_{osc}C_c+2\Delta\omega C}{\omega_{osc}C_c+4\Delta\omega C}\right]^2\frac{2}{V_a^2}$$
$$=\frac{1}{2}F\frac{\overline{i_{nR}^2}}{\Delta f}\left|Z_r(\mathrm{j}\omega)\right|^2\frac{1}{V_a^2} \tag{6.8}$$

The phase noise for the standalone oscillator is given by

$$F\frac{\overline{i_{nR}^2}}{\Delta f}\left|Z_r(\mathrm{j}\omega)\right|^2\frac{1}{V_a^2} \tag{6.9}$$

From (6.8) and (6.9) it is seen that power combining results in a 3-dB phase noise reduction independent of the offset frequency $\Delta\omega$. A representative simulated phase noise plot for the coupled oscillator is shown in Fig. 6.5. In general, capacitively coupling N oscillators improves phase noise by $10\times\log_{10}(N)$ dB.

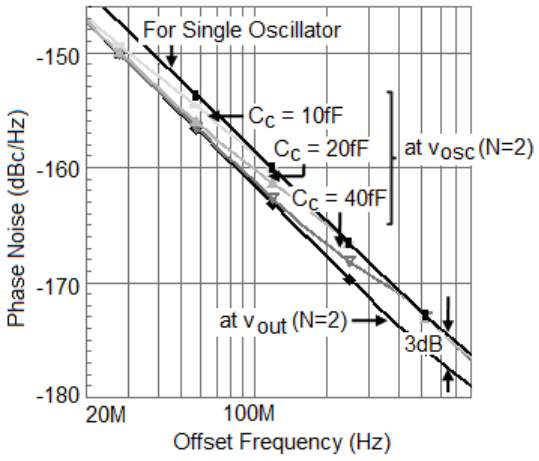


Figure 6.5: Phase noise of coupled LC oscillator

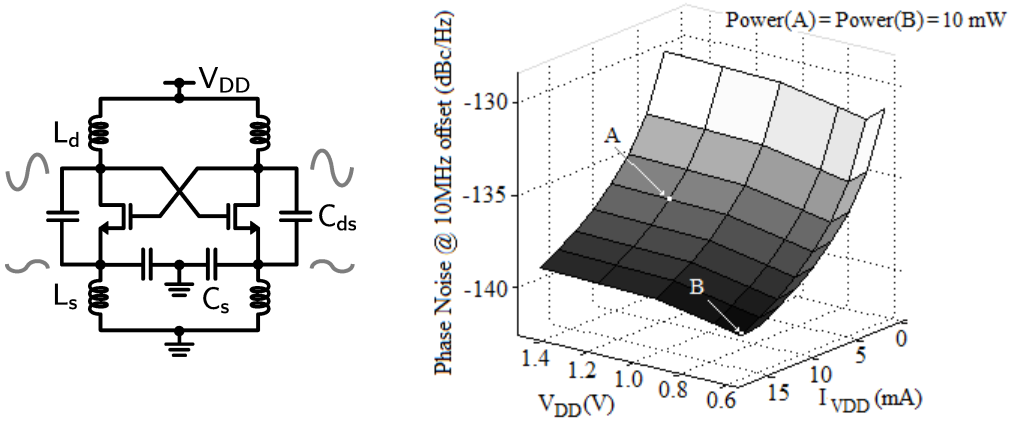
6.2.4 Design Tradeoffs in Choice of Coupling Capacitance

From the above analyses, we infer that increasing C_c helps in suppression of spurious modes that can arise due to high order resonances of the load of the oscillator. This enforces the in-phase locked operation. Moreover, simulations reveal that an insufficiently large C_c would limit the amount and bandwidth of phase noise reduction in the presence of mismatch between the oscillator cores or coupling paths to the output. The effect of coupling path mismatch in the limiting case where the phase noise is observed directly at output of one of the core oscillators and its dependence on C_c is captured in the simulated plots of Fig. 6.5. Increasing C_c also reduces the signal attenuation caused by the voltage divider formed by the capacitive coupling network and the input impedance of the buffer.

Too large a value of C_c however, reduces the tuning range due to larger substrate parasitics from C_c. These constraints are used to determine the optimal value of C_c for the design.

6.3 Current Reuse

If the supply voltage is increased in an oscillator at a given bias current, the oscillation amplitude can be correspondingly made larger by increasing the tank impedance, in order to decrease phase noise. This allows for a trade-off between phase noise and power dissipation . Beyond a certain value of the output swing, however, the phase noise degrades as the active devices of the oscillator can enter into the triode region for part of the cycle. The oscillation



(a) (b)

Figure 6.6: Low voltage oscillator (a) Schematic [52] (b) Noise vs. $\{V_{DD}, I_{VDD}\}$

amplitude can also be limited by reliability considerations. With a sufficiently large power supply and output swing, the phase noise of an oscillator is thus determined primarily by the bias current. Consequently, when the system supply is significantly larger than the value required for minimizing phase noise per unit power, current-reuse reduces phase noise with little or no increase in DC power.

Several VCO topologies reported in the literature (*e.g.* [39][40][51]) employ a bias current transistor and therefore have a relatively large power supply voltage requirement. An oscillator topology (Fig. 6.6(a)) which does not employ a bias current transistor and operates at low voltage was reported in [52]. This implementation achieves low phase noise due to the large voltage swing established by capacitive feedback from the drain to source of the core devices. Fig. 6.6(b) shows a representative simulated variation of phase noise

with supply voltage (V_{DD}) and current (I_{VDD}) in such a topology.

In our work we employ the operating principle of this topology. Two stacked oscillators that reuse the bias current are connected in series. This exploits the weak tradeoff between noise and V_{DD} mentioned above. Capacitive power combining is employed to achieve low phase noise at negligible power overhead compared to conventional LC oscillators. Most systems at this process node employ a low voltage power supply of approximately 1.5 V that is regulated down with an Low Drop-out regulator and naturally lends itself to this current reuse topology.

6.4 Design Implementation

6.4.1 Voltage Controlled Oscillator

A simplified schematic diagram of the oscillator is shown in Fig. 6.7. It consists of four low-voltage oscillator cores [52] that employ two current reuse stacks. One such oscillator core is indicated in the figure. PMOS transistors, *e.g.* M_{P1} and M_{P2}, are used for implementing the cross-coupled switching pairs because they have a lower $1/f^3$ noise corner than an NMOS implementation [53]. The body potential of the switching transistors is chosen nominally to be 0.33 V (V_b) and 0.98 V (V_t), in order to reduce the threshold voltage and supply requirement without degrading phase noise. The inductors (L_d and L_s) and capacitors (C_{ds} and C_s) comprise the energy storing passive network. Each stack of two oscillator cores is biased by controlling the supply which is nominally held at 1.3 V through a voltage regulator. In each stack, the

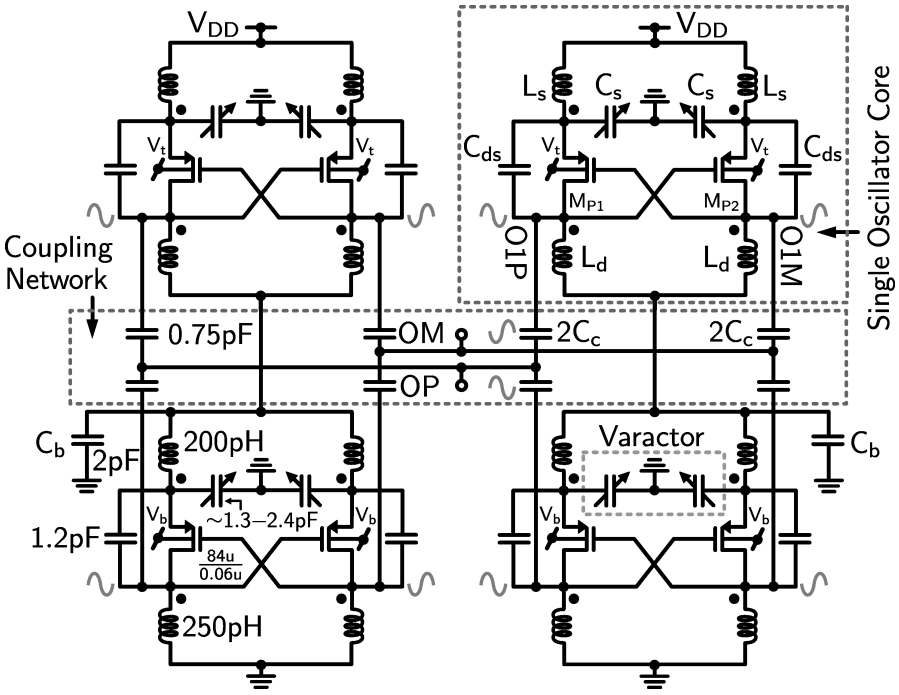


Figure 6.7: Two-way stacked capacitively coupled oscillator

intermediate node between top and bottom oscillators is grounded at high frequency by using a bypass capacitor (C_b).

The differential outputs of each of the four oscillator cores, *e.g.*, $O1P$ and $O1M$, are coupled to the output nodes, OP and OM, of the power combined oscillator through identical capacitors ($2C_c$). The resulting coupling network is marked in Fig. 6.7. Frequency tuning is achieved by varying the source capacitors (C_s) simultaneously for all oscillators. C_s consists of a combination of discretely tuned, switched metal-insulator-metal capacitors, in parallel with continuously tunable varactors.

A layout approach that helps reduce area [54] is employed. A two-turn

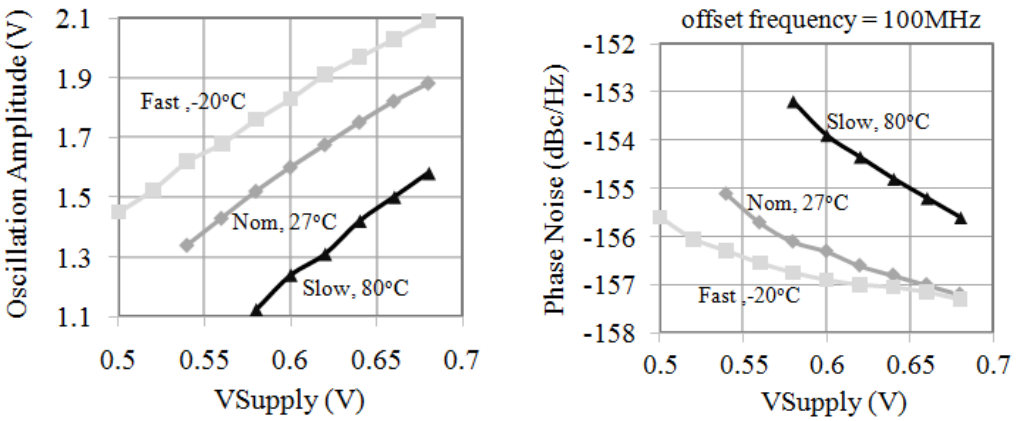
inductor (L_s) is placed within a single-turn inductor (L_d) of similar value with low mutual inductance as seen in the die photo in Fig. 6.14. For our choice of inductor values, the coupling coefficient obtained from EM simulations was 0.16. The simulated phase noise degraded by about 0.3 dB due to the lower Q of the two-turn inductor (L_s).

The oscillator is buffered with an open drain, on-chip amplifier which drives a differential 100 Ω load established by the measurement equipment and a 50 Ω termination resistor. The buffer is designed to ensure that its noise floor does not mask the phase noise of the oscillator up to an offset frequency of several hundred MHz.

6.4.2 Supply Regulation

In the low voltage oscillator the supply magnitude as well as process dependent device parameters like threshold voltage determine the output swing (Fig. 6.8(a)). Moreover, this sets the phase noise (Fig. 6.8(b)) since the current is dependent on the swing in the absence of any tail current source. To make the topology robust against PVT variation the oscillator is thus embedded in a digitally assisted amplitude control loop, similar to [55]. The reference of an LDO providing the supply of the oscillator is controlled to achieve an externally programmed amplitude. This not only ensures robust startup but also, as can be observed from the figures, reduces the phase noise variation significantly. The simplified control loop in shown in Fig. 6.9. A peak detector converts the amplitude information into a DC voltage and it is

compared against voltage corresponding to desired oscillation amplitude which is programmed using a current DAC. The dummy peak detector shown serves as a reference and helps reducing process dependent offset error which arises if only a standalone peak detector is used. The comparator output controls an finite state machine (FSM) which governs the direction in which the LDO reference, controlled by a scaling RDAC, and hence the oscillator supply needs to be changed. The FSM uses binary search algorithm to minimize number of steps in the process of settling to correct supply value. A switched LPF is placed at the RDAC output to filter the additive noise from the control loop. To ensure fast settling, the LPF cutoff frequency is set dynamically to a sufficiently high value when amplitude loop is in action and a low value after steady state is reached. The loop elements are powered down after the oscillation amplitude stabilizes in order to avoid any power penalty from them.



(a) (b)

Figure 6.8: Low voltage oscillator (a) PVT sensitivity of amplitude (b) PVT sensitivity of phase noise

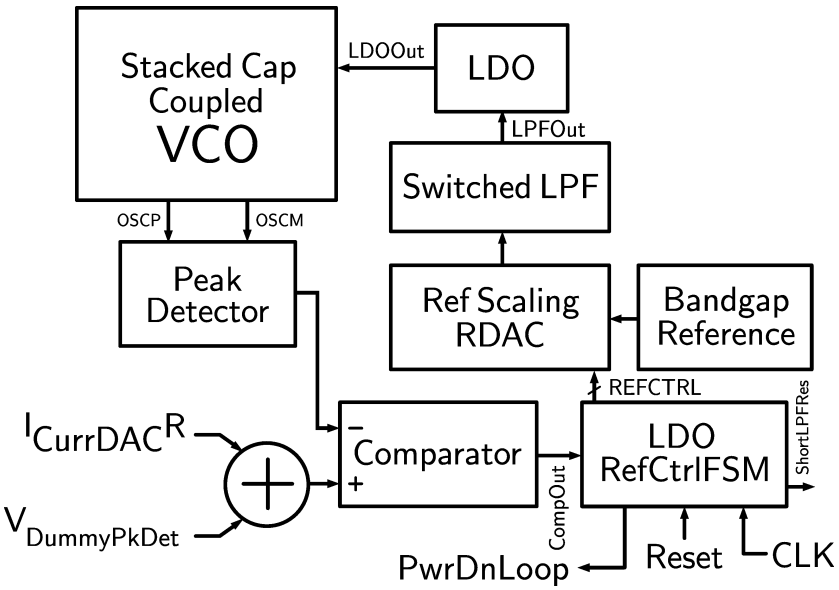


Figure 6.9: Control loop used for supply regulation

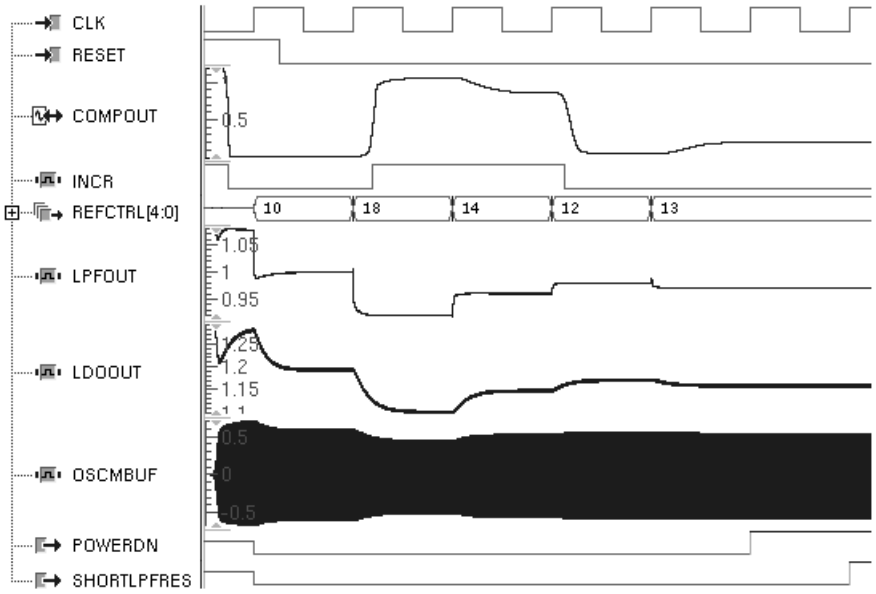


Figure 6.10: Simulated waveforms appearing at nodes within control loop

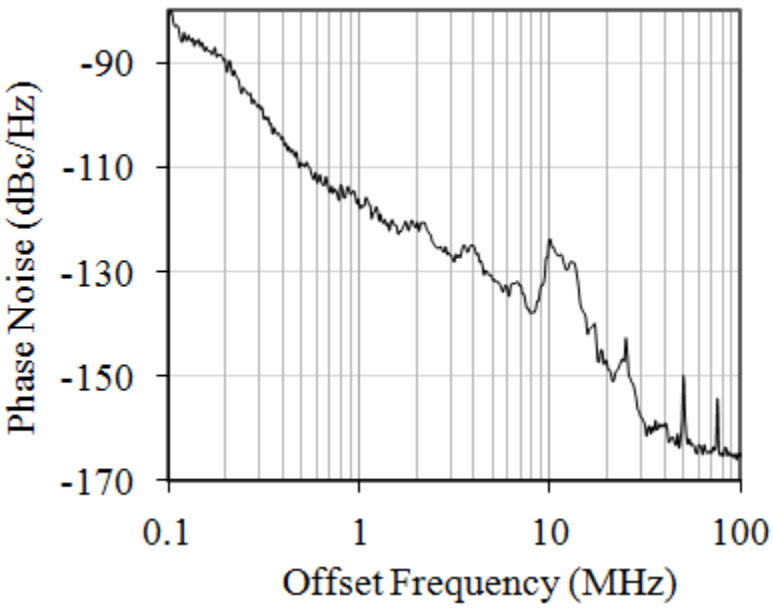


Figure 6.11: Measured phase noise at 10 GHz oscillation frequency

The simulated waveforms at different points within this control loop are shown in Fig. 6.10.

6.5 Experimental Results

The oscillator was implemented in a 7-metal, 45 nm CMOS process (Fig. 6.14) and has a core area of 0.67 mm^2. The performance of the VCO was measured on-wafer using an Agilent E5052A signal source analyzer and E5053A downconverter. Fig. 6.11 shows the measured phase noise plot for an oscillation frequency of 10GHz. The phase noise at 20 MHz offset was -148.7 dBc/Hz. The oscillator consumed 22.6 mA from a 1.3 V supply. The signal source analyzer was only capable of measuring phase noise at an offset up

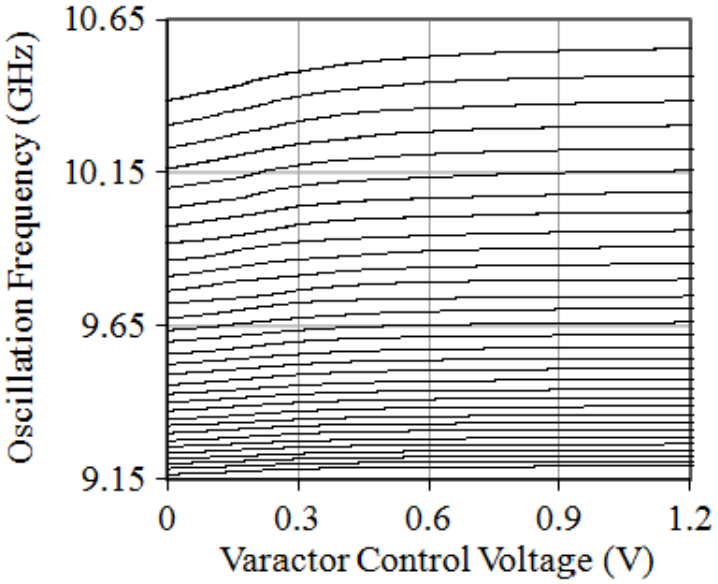


Figure 6.12: Measured tuning curves for the VCO

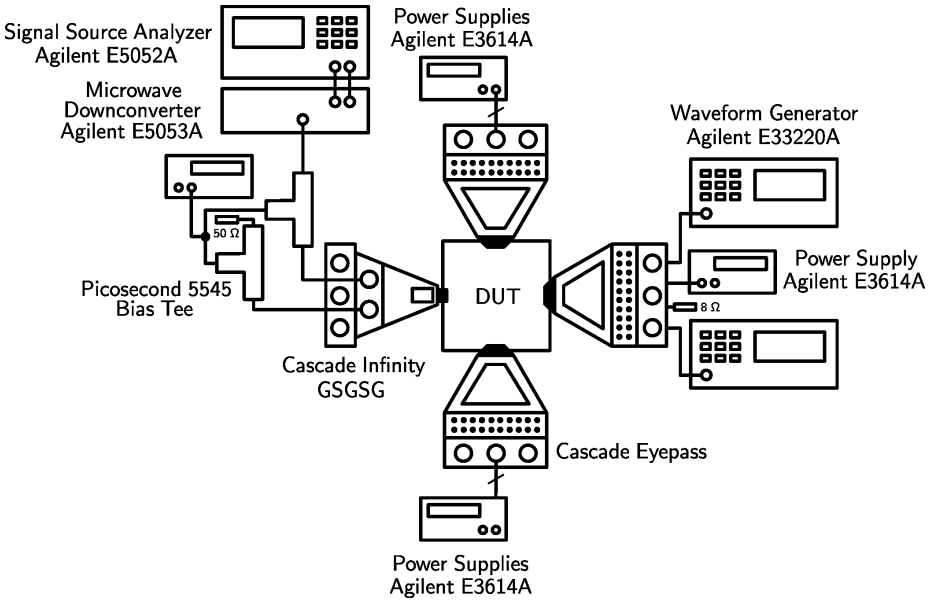


Figure 6.13: VCO measurement setup

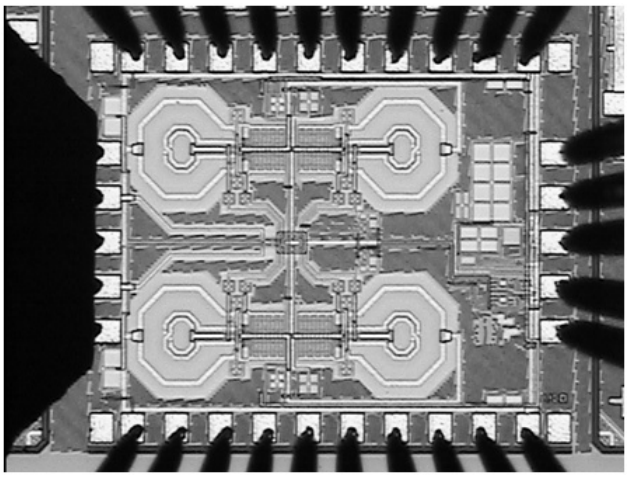


Figure 6.14: Die micrograph of the VCO

to 100 MHz. Simulations show the phase noise decreases to less than -182 dBc/Hz at 1 GHz. The peaking at 10 MHz offset was caused by coupling from the data link clock employed to communicate with the setup.

The Figure of Merit (FOM) for oscillators is commonly expressed as

$$FOM = 10\ \log_{10}\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}P_{DC,mW}}\right] \tag{6.10}$$

where f_0 is the operating frequency, Δf is the offset frequency, $L\{\Delta f\}$ is the phase noise at offset Δf and $P_{DC,mW}$ is power dissipated in mW. The FOM of our oscillator evaluated at an offset of 20 MHz is 188. The oscillator exhibits a tuning range of 9.15-10.6 GHz (Fig. 6.13). The FOM, considering the fractional tuning range, is 191.3. This VCO is targeted for application in the 2.4-2.5 GHz band of WiFi/WiMax/Bluetooth. The measurement setup is shown in Fig. 6.13. A low noise divider ($\div 4$) can be used for deriving the

LO for such applications. This would lower the phase noise by up to 12 dB, while maintaining high sensitivity when one radio coexists in close spectral proximity to another.

The performance of our VCO is seen to compare favorably with or exceed that of other recently reported multi-GHz VCOs (Table 6.1).

6.6 Conclusion

A low phase noise VCO with a tuning range from 9.15 to 10.6 GHz has been presented. Capacitive coupling of multiple oscillators achieves a phase noise of -148.7 dBc/Hz at 20 MHz offset while dissipating 30 mW from a 1.3 V supply in 45 nm CMOS. The low far-out phase noise performance reduces reciprocal mixing from in-band blockers, which can appear at offsets of several MHz, for coexisting and collocated radios.

Table 6.1: VCO Performance Comparison

Ref.	Tuning Range(GHz)	Power (mW)	PN(dBc/Hz) @offset(Hz)	FOM	CMOS Tech.†
[56]	8-12	27	-127@10M	172.7	130nm
[57]	4.39-5.26	6.3	-132@10M	177.7	180nm
[46]	15.4-16.3	8.1	-127@10M	182.0	180nm
[58]	4.28-5.33	3	-134@10M	183.0	130nm
[59]	16.8-17.6	12.2	-134@10M	188	BiCMOS
[60]	12.2-12.6*	2.2	-132@10M	190.5	180nm
[61]	4.57-5.83	3.9	-141@10M	189.4	180nm
This Work	9.15-10.6	30	-149@20M	188	45nm

*High Frequency Mode †Unless mentioned otherwise

Chapter 7

Growth of Oscillation in a Multi-Mode Quadrature Oscillator

7.1 Introduction

In the last chapter we discussed a capacitively coupled oscillator topology and the potential for multi-mode oscillation in it. Multi-mode oscillations can arise in many other contexts, *e.g.*, oscillators which synthesize multiphase outputs, injection locking and pulling between oscillators, and oscillators for multi-band standards. The growth of oscillation in such oscillators is important to analyze since it can guide design choices required to prevent erroneous signal processing which can potentially occur if a wrong mode is selected in the steady state. In the previous chapter we briefly mentioned the role played by cross-compression amongst competing modes in our proposed oscillator for suppression of modes with smaller loop gain. It was also noted strong coupling established by a large coupling capacitor can be used to introduce the necessary growth-rate asymmetry to ensure that the desired mode is dominant.

In this chapter we perform a detailed analysis of this cross-compression mechanism for mode selection. We consider the problem of a multi-mode quadrature oscillator whose coupling path consists of a combination of active

and passive devices as a case study. The analysis approach can be adapted to topologies using other forms of coupling, *e.g.*, in our capacitively coupled oscillator, by suitably modifying the expressions for mode frequencies, phase relationships and system equations described below to take into account the change in the coupling network parameters.

Quadrature oscillators are used extensively for frequency synthesis in modern communication systems, *e.g.* as LOs in direct-conversion receivers and clocks for CDR systems. Fig. 7.1 shows a conventional quadrature oscillator topology [62] consisting of two oscillator cores along with differential transistor pairs, *e.g.* (M_{ipz}, M_{imz}), that couple the cores. The design has two stable[1] oscillation modes with complementary phase ordering [63][64]. These two modes also vary in terms of the polarity of frequency shift relative to the resonant frequency of the tank. Both modes can be shown to have a similar startup rate, and therefore for achieving predictable operation, it is necessary to ensure *a priori* that only one of them survives in steady state. Adding phase shift in the coupling-path produces asymmetry in the startup rates and achieves this. The desired phase shift can be realized through reactive degeneration of the coupling transistors using impedance Z_d as shown in the figure.

Here, we demonstrate an analytical solution for the temporal evolution of oscillation in the above oscillator, by presenting an explicit solution for

[1]A mode of oscillation is defined to be stable if the oscillator returns to the initial equilibrium state corresponding to that mode after being subjected to some arbitrarily small perturbation.

the system differential equations. This solution takes into consideration the above-mentioned modes that can exist at the startup of oscillation. In addition we explain how the dominant mode, which is the one with highest growth-rate, of oscillation is determined by the phase shift provided by the reactively degenerated coupling circuits and the impact of cross-compression on mode selection. The degeneration impedance (Z_d) is synthesized using inductor L_d or a parallel combination of a large inductance that provides a path for the bias current and capacitance (C_d). The parallel $L-C$ is used at a frequency greater than its shunt resonance frequency, so that it effectively provides capacitive degeneration impedance of $1/(sC_d)$. The two types of degeneration provide phase-shifts with different polarities in the coupling paths.

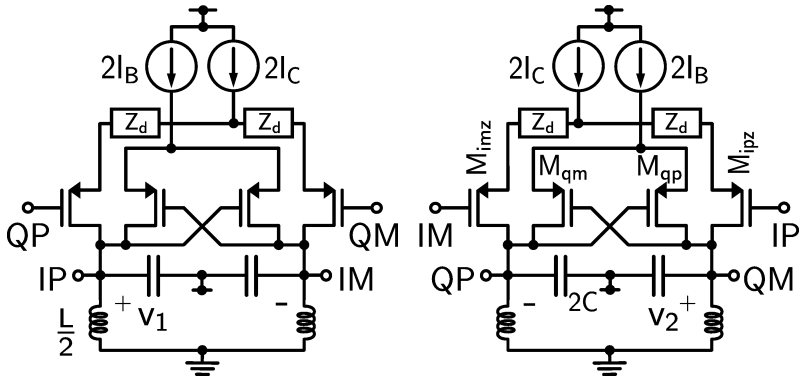


Figure 7.1: Schematic of the quadrature oscillator (Z_d is a short in [62])

7.2 Analysis of Growth of Oscillation

7.2.1 Overview

The coupled-core based oscillator is assumed to employ reactively degenerated coupling path transistors, that have four possible modes of oscillation for any phase shift γ that is provided by the coupling path.. However, only two of these modes are stable and produce quadrature outputs. The other two modes have been shown to be unstable using perturbation analysis [65] and are not considered here.

The build-up of oscillation is discussed in Subsection 7.2.2, where we employ small signal modeling to evaluate the oscillation frequencies for the two stable modes. The evaluation of the relevant non-linear coefficients for analyzing large signal behavior under assumptions of weak non-linearity is discussed in Subsection 7.2.3. These parameters are used in Subsection 7.2.4 where we assume that the quadrature oscillator node voltages are given by the superposition of the two modes at frequencies calculated through linear analysis. The differential equations governing the system are set up and solved to determine the evolution of amplitude and phase in the two modes. The authors of [66] analyzed the dynamics of an oscillator that employed a single negative resistance core loaded with a high order resonator using similar techniques. This is in contrast to the class of coupled oscillator cores which we address here. An analysis of quadrature oscillators with phase shifters was presented in [64] and [65]. However, a solution to the system differential equations and an analysis of the mode suppression mechanism were not provided. In Subsection 7.2.5

we present physical insights into the behavior of the oscillator based on the above analyses.

7.2.2 Small Signal Modeling

We represent the differential transconductance of the transistors comprising the negative-resistance cores, *e.g.* (M_{qp}, M_{qm}), by a_1. The real and imaginary components of effective differential transconductance $\boldsymbol{a_{1c}}$ of the coupling transistors, *e.g.* (M_{ipz}, M_{imz}), that include the effect of reactive degeneration are denoted by a_{1cr} and a_{1ci} respectively. The frequency dependence of $\boldsymbol{a_{1c}}$ is ignored since the dependence is expected to be weak over the frequency range of interest. Its value is evaluated at $\omega_r = \frac{1}{\sqrt{LC}}$ where L and C are the tank inductance and capacitance respectively. In terms of coupling-path phase shift γ and magnitude of coupling transconductance, $a_{1c} \equiv |\boldsymbol{a_{1c}}|$, we have, $a_{1cr} = a_{1c}\cos\gamma$ and $a_{1ci} = -a_{1c}\sin\gamma$. It is assumed that $|a_{1ci}|$ is much smaller than a_1, which is the case for typical bias and sizing. Further, we assume $|\gamma| \leq 90^\circ$ as is the case for typical values of degeneration impedance.

In the two stable modes, the phase difference $\Delta\phi$ between the in-quadrature single-ended nodes *e.g.* $\phi_{QM} - \phi_{IP}$ is either +90° or -90°. We denote the case of $\Delta\phi$ = -90°, as *mode*-1 (m_1) and the other possible phase difference $\Delta\phi$ = +90°, as *mode*-2 (m_2). Assuming an unstable equilibrium in presence of small signals and using above criterion for $\Delta\phi$, it can be shown that the oscillation frequencies of two aforementioned modes are

$$\omega_{1,2} \;=\; \omega_r \left(1 \mp \frac{1}{2Q_{reso}} \frac{a_{1c}\cos\gamma}{a_1 \mp a_{1c}\sin\gamma}\right) \tag{7.1}$$

where $Q_{reso} = R_{tank}/(\omega_r L)$. It can be seen that $\omega_1 < \omega_2$. The above results give us the initial frequency and phase ordering ($\Delta\phi$) for each mode. It is noted that the oscillation frequencies are only weakly sensitive to exact initial condition and associated large signal behavior. The amplitude ratio between the in-phase (I) and quadrature (Q) cores is unity for the stable modes due to symmetry. The mode superposed voltages represent the solution for the system equations.

7.2.3 Evaluation of Non-linear Coefficients

The buildup of oscillation leads to an increase in the amplitude of non-linearity induced signals. During the initial growth of oscillation, the transistors operate in weakly non-linear class-A mode. Consequently we employ the weakly non-linear Van der Pol model for the coupled oscillator. The cross-coupled core and the coupling pair transistors are both assumed to exhibit 3^{rd}-order non-linearity, while higher order non-linearity is neglected. It is noted that the analysis is valid *even* if the steady state amplitude is large enough to eventually cause complete current commutation, since the dominant oscillation mode is determined during the startup phase itself.

Approximate linear and cubic coefficients for the negative resistance cores (a_1 and a_3 respectively) are determined by fitting the non-linearity of the polynomial model to the V-I characteristics of the differential pair. These coefficients are broadband since all their device parasitics can be absorbed as part of the tank capacitance to the first order.

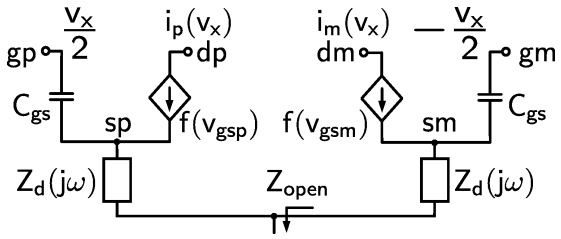


Figure 7.2: Model for non-linearity analysis of coupling transconductors

To evaluate the non-linear coefficients for the reactively degenerated coupling pair we utilize the Volterra series analysis and use the model shown in Fig. 7.2. The reactive degeneration impedance is denoted by $Z_d(s)$ and it equals either sL_d or $1/sC_d$. C_{gs} is the effective MOS gate-to-source capacitance. Coefficients a_{id}, for $i = 1$ to 3, are used to represent the non-linearity of the MOS transistors that are degenerated to achieve phase shift. These coefficients are estimated by fitting the DC transconductance characteristic. Using this model we can evaluate, as shown in Appendix D, the coefficients $C_1(s)$and $C_3(s_a, s_b, s_c)$ that express the device currents as functions of the voltage across the tank load.

7.2.4 Solution of the System Differential Equations

In solving the system equations we use the Kryloff Method of First Approximation, which replaces functions of slowly varying quantities by their respective time-averaged values, under assumption of quasiharmonic oscillation [67].

The differential equations governing the system model of the coupled oscillators (Fig. 7.3) are

$$\frac{v_1}{L} + C\dot{v_1} + G\dot{v_1} - (a_1\dot{v_1} + 3a_3v_1^2\dot{v_1}) - \frac{\mathrm{d}}{\mathrm{d}t}(C_1(\omega) \circ v_2 + C_3(\omega_a, \omega_b, \omega_c) \circ v_2^3) = 0 \tag{7.2a}$$

$$\frac{v_2}{L} + C\dot{v_2} + G\dot{v_2} - (a_1\dot{v_2} + 3a_3v_2^2\dot{v_2}) + \frac{\mathrm{d}}{\mathrm{d}t}(C_1(\omega) \circ v_1 + C_3(\omega_a, \omega_b, \omega_c) \circ v_1^3) = 0 \tag{7.2b}$$

where v_1 and v_2 are the differential voltages across tanks, and $G(\equiv 1/R_{tank})$ is the effective conductance of tank load evaluated at ω_r. The mode-superposed differential quadrature node voltages are,

$$v_1 = \alpha_1 \cos\theta_1 + \alpha_2 \sin\theta_2 \tag{7.3a}$$

$$v_2 = \alpha_1 \sin\theta_1 + \alpha_2 \cos\theta_2 \tag{7.3b}$$

$$\theta_i = \omega_i t + \phi_i \tag{7.4}$$

where $i \in [1, 2]$, α_i and θ_i are instantaneous amplitude and phase respectively in i^{th} mode. The frequencies ω_i's are given by (7.1) and ϕ_i's are slowly varying components of instantaneous phases in the two modes. We represent $v_1(t)$, $v_2(t)$, $\alpha(t)$, $\theta(t)$ and $\phi(t)$ by v_1, v_2, α, θ and ϕ respectively, where time dependence is implicit. All other physical quantities are time-invariant.

These equations are solved in Appendix E to obtain the following state equations (7.5) that govern the evolution of oscillation in the quadrature oscillator.

$$\dot{\alpha_1} = \frac{\omega_1\alpha_1}{\omega_1 + \omega_2}\frac{1}{C}\{-G + a_1 - a_{1c}\sin\gamma + \frac{3}{4}(\alpha_1^2 + 2\alpha_2^2)(a_3 + a_{3ci})\}$$

$$\dot{\alpha_2} = \frac{\omega_2\alpha_2}{\omega_1 + \omega_2}\frac{1}{C}\{-G + a_1 + a_{1c}\sin\gamma + \frac{3}{4}(\alpha_2^2 + 2\alpha_1^2)(a_3 - a_{3ci})\}$$

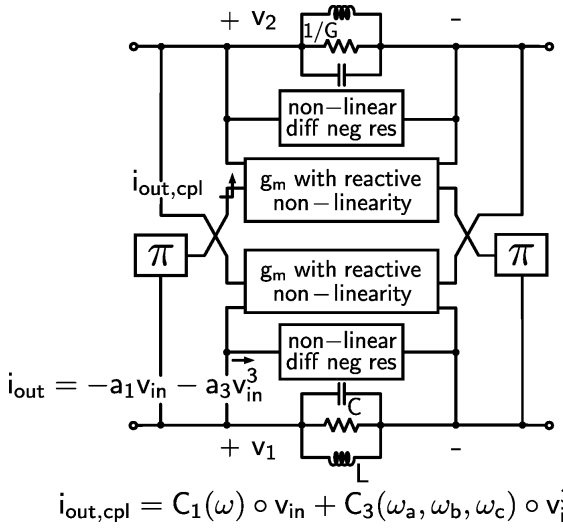


Figure 7.3: Quadrature oscillator model used in derivation

$$\dot{\phi}_1 = -\frac{1}{\omega_1+\omega_2}\{\omega_1^2 - \omega_r^2 + \frac{\omega_1}{C}(a_{1c}\cos\gamma + \frac{3}{4}a_{3cr}(\alpha_1^2 + 2\alpha_2^2))\}$$
$$\dot{\phi}_2 = -\frac{1}{\omega_1+\omega_2}\{\omega_2^2 - \omega_r^2 - \frac{\omega_2}{C}(a_{1c}\cos\gamma + \frac{3}{4}a_{3cr}(\alpha_2^2 + 2\alpha_1^2))\} \quad (7.5)$$

where,

$$a_{3cr} = |C_3(\omega_r, \omega_r, -\omega_r)|\cos\angle C_3(\omega_r, \omega_r, -\omega_r)$$
$$a_{3ci} = |C_3(\omega_r, \omega_r, -\omega_r)|\sin\angle C_3(\omega_r, \omega_r, -\omega_r)$$

The first two equations in (7.5) capture the time evolution of oscillation amplitude. Steady state values of amplitude and frequency can be obtained by solving these equations.

7.2.5 Observations

Based on the above analysis, we can make several observations regarding the working principle of the oscillator under assumptions of noise-initiated startup. For a positive phase shift of the coupling-path differential pairs, γ,

which is the case for inductive degeneration, from (7.5), *mode*-2 with frequency ω_2 is seen to be dominant, i.e., that is it has a greater initial growth factor $T_2 \equiv \exp\{\omega_2/(C(\omega_2+\omega_1))(-G+a_1+a_{1c}\sin\gamma)t\}$ compared to *mode*-1 which has a growth factor of $T_1 \equiv \exp\{\omega_1/(C(\omega_2+\omega_1))(-G+a_1-a_{1c}\sin\gamma)t\}$. For capacitive degeneration (*i. e.* negative γ), *mode*-1 is dominant ignoring the range of small γ magnitudes where the factor $\omega_2/(\omega_1+\omega_2)$ plays a role. Therefore, we can conclude that the *polarity* of γ decides the dominant mode.

To understand the dependence of mode suppression on the magnitude of γ we assume a positive value of γ, without loss of generality. The initial values of α_1 and α_2 are α_{1init} and α_{2init} respectively. κ is defined as the initial-condition skew factor and is given by $\alpha_{1init}/\alpha_{2init}$.

We first consider the case of $\kappa \approx 1$. This is relevant in the practical case for which the noise power levels at the two possible oscillation frequencies, ω_1 and ω_2 is at similar levels. From the state equations (7.5) we then see that non-dominant mode growth in amplitude is governed by a factor

$$(-G+a_1-a_{1c}\sin\gamma+\frac{3}{4}(a_3+a_{3ci})(\alpha_1^2+2\alpha_2^2))\alpha_1 \tag{7.6}$$

The terms $G\alpha_1$ and $a_1\alpha_1$ are related to the tank resistance and negative resistance provided by the cross-coupled cores respectively. $a_{1c}\alpha_1\sin\gamma$ arises from the coupling transistors. $\frac{3}{4}(a_3+a_{3ci})\alpha_1^3$ is due to self-induced compression and $\frac{3}{2}(a_3+a_{3ci})\alpha_2^2\alpha_1$ is from the dominant mode induced compression. Due to a lower starting growth-rate for the non-dominant mode, α_1 will decrease compared to α_2 at an exponential rate and become negligible within several cycles

after startup. Therefore we can ignore the self-induced compression term in (7.6) and approximate it by

$$(-G + a_1 - a_{1c}\sin\gamma + \frac{3}{2}(a_3 + a_{3ci})\alpha_2^2)\alpha_1 \tag{7.7}$$

From the above expression we observe that the dominant mode induced compression suppresses the growth of oscillation. Moreover, since in the steady state, the dominant mode amplitude is constant, *i. e.*,

$$(-G + a_1 + a_{1c}\sin\gamma - \frac{3}{4}(|a_3| + a_{3ci})\alpha_2^2) = 0 \tag{7.8}$$

the non-dominant mode will be attenuated due to an amplitude growth rate that is negative under typical condition of $|a_3| \gg |a_{3ci}|$. The non-dominant mode will be suppressed with time, even if it starts up, due to this compression induced ordering of the growth rates. The rate of suppression is greater with larger $|\gamma|$ due to an increase in the difference of the initial growth-rate of oscillation. For sufficiently positive values of γ, as we will see below, points in the phase portrait with $\kappa \gg 1$ are in the region of attraction (ROA) [68] of the equilibrium point corresponding to dominant *mode*-2. This ensures that the process is not sensitive to noise induced uncertainties of the exact initial condition.

The oscillation frequencies of the modes, in the unphysical case that both modes reach steady state, are obtained from (7.4) and (7.5) as $\omega_1 + \dot{\phi}_1$ and $\omega_2 + \dot{\phi}_2$. Since $|\dot{\phi}_i| \ll \omega_i$ and $|\omega_2 - \omega_1|$ for $i = 1, 2$, the mode frequencies can be approximated as ω_1 and ω_2.

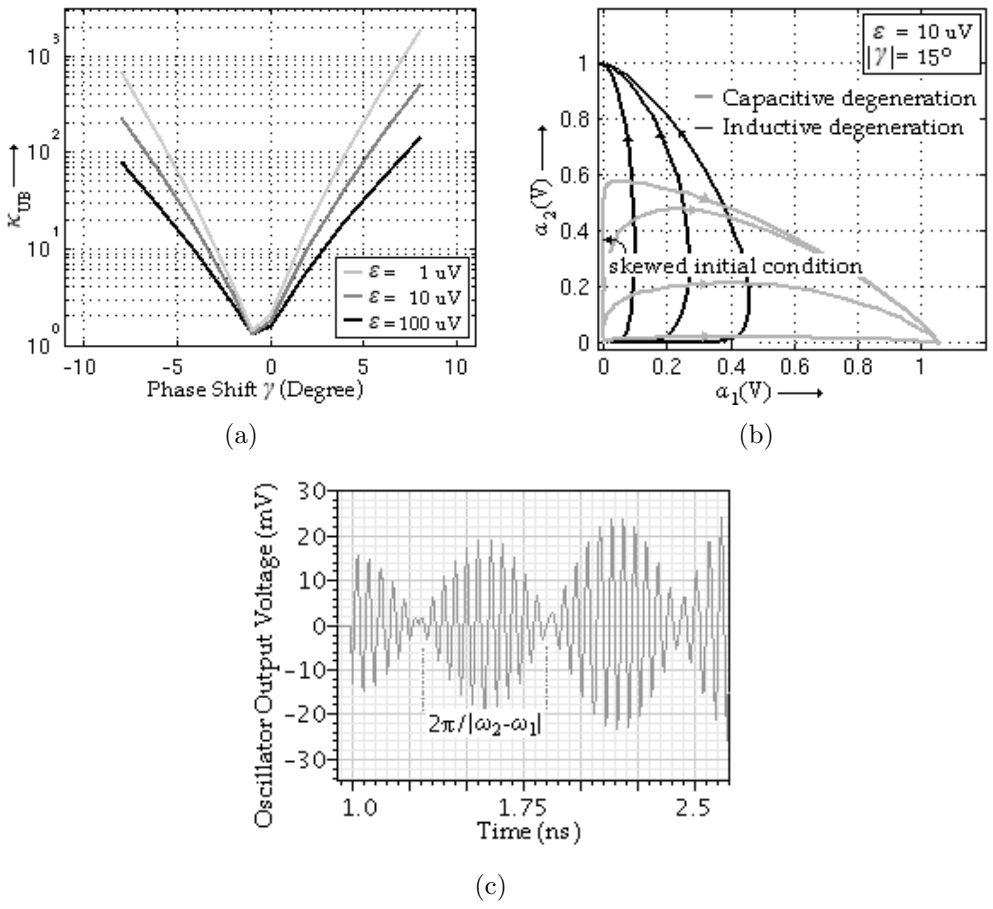


Figure 7.4: Simulated results (a) Skew factor(κ) upper bound for ROA of dominant mode's equilibrium point as f(ε,γ) (b) Oscillator phase portrait under skewed initial conditions (c) Evanescent beats produced by competing modes at startup

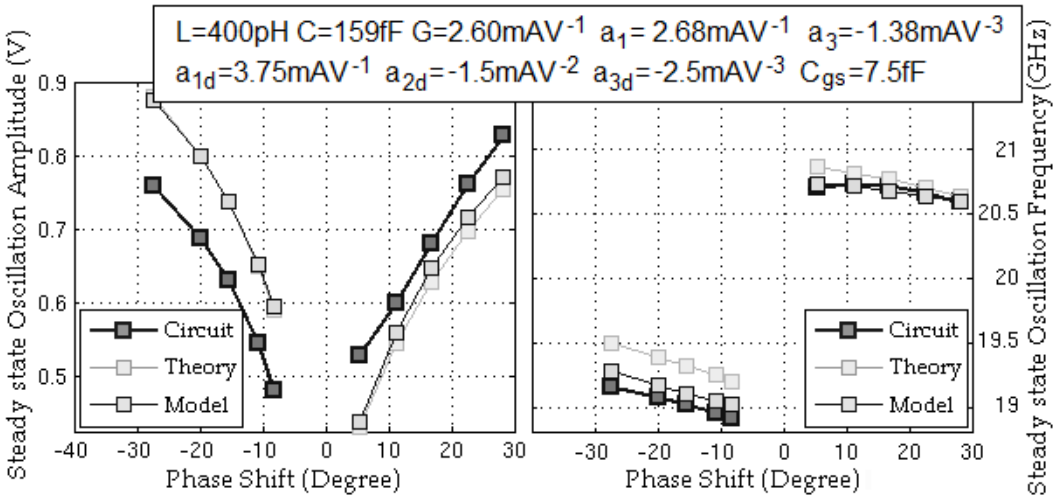


Figure 7.5: Comparison of steady state oscillation amplitude and frequency

7.3 Simulation Results

Simulation results for a quadrature oscillator designed in a 0.13-μm CMOS technology and its associated mathematical model are shown in Fig. 7.4(a) through Fig. 7.4(c). Fig. 7.4(a) shows κ_{UB}, which is the upper bound of κ for the ROA of the dominant mode's equilibrium point, as function $f(\epsilon, \gamma)$ of its initial amplitude (ϵ) and phase shift (γ). It can be observed that for $|\gamma| \geq \gamma_{min}$ and $\epsilon \leq \epsilon_{max}$ we have $\kappa_{UB} \geq \min\ f(\epsilon_{max}, \pm\gamma_{min})$. For example, if $\gamma_{min} = 7.5°$ in the implementation and $\epsilon_{max} = 0.1$ mV, then the above-mentioned ROA has a $\kappa_{UB} \geq 50$. The physical significance of this observation is that for noise initiated startup, which determines the value of ϵ, the non-dominant mode can have an initial amplitude gain ($=\kappa$) as large as 50 but the system will still successfully suppress it and converge to the other mode.

Since κ is related to the ratio of noise in the two oscillation modes, in practice it will have a value significantly smaller than this, and therefore the dominant mode is guaranteed to be selected. Fig. 7.4(b) shows a representative phase portrait obtained using (7.5) in the two types of degeneration under skewed initial conditions for $|\gamma| = 15^\circ$ and noise-initiated startup, *e.g.* $\epsilon = 10$uV. The mode suppression phenomenon is captured in the transient response shown in Fig. 7.4(c), as initial beats occurring due to the co-existence of the two modes. Since one of the modes begins to dominate over time, the beats decay, eventually leading to oscillation at the frequency of the dominant mode. The steady state amplitude and frequency predicted by (7.5) and (7.1) (labeled Theory) and the results from representative implementations with different values of γ (labeled Circuit) are shown in Fig. 7.5. The results, labeled Model, are obtained by directly simulating the system model described by equation (7.2) and thus capture effects due to the use of quasiharmonic assumption and the Method of First Approximation. The estimated parameters used for Theory and Model are shown in the inset. The term G, in equation (7.5), is estimated from the Q of the passives and the finite output impedance (g_{ds}) of the transistors. The results show agreement in trends and maximum amplitude error of approximately 20% between theory and implementation. The deviation in amplitude can be attributed to the error in the accurate estimation of the value of G and higher-order effects such as the non-linearity of the output impedance and capacitance of the devices.

7.4 Conclusions

The time evolution of oscillation in a quadrature oscillator has been analyzed. Quasiharmonic assumption and the Method of First Approximation are used starting with mode superposed node voltages, to demonstrate convergence to one of two possible stable oscillatory modes. Compression induced by the dominant mode is shown to suppress the non-dominant mode. The magnitude of the phase shift, provided by the reactively degenerated coupling path transistors, is shown to control rate of suppression of the non-dominant mode. The polarity of phase shift determines the oscillation frequency. Close agreement is seen between the theoretical predictions and simulated results for steady state oscillation frequency and amplitude. Similar analysis techniques are applicable to other multi-mode multiphase oscillator topologies and also to coupled multi-mode oscillators.

Chapter 8

Conclusions

8.1 Review

Power efficiency has become a major consideration in the design of radio front-ends. This metric is especially significant in applications such as wireless personal area networks, telemetry and sensor networks, and is also becoming increasingly important due to the progressively greater complexity of wireless transceivers.

In first part this work low-power dynamic-range optimized receiver was proposed for such applications. The receiver employs a down-converter core which simultaneously reuses bias current and shares the power supply domains between RF and baseband stages. Such a sharing offers significant advantage with respect to available headroom over prior work on current-sharing, that relies on stacking of multiple sub-blocks. The RF transconductance stage and the baseband transimpedance amplifier which are coupled through a passive current-mode mixer each play a dual role, while the impedance translation property of the mixer core ensures the desired signal flow. The dynamic range of the basic topology is further enhanced by using active noise suppression. This is achieved through the use of active negative resistances, which increase

the effectiveness of intrinsic feedback elements, series-series and shunt-shunt, in suppressing low-frequency noise. A technique to linearize the baseband transimpedance stage by using non-linear feedback has also been demonstrated. It is noted that the use of transresistance to provide gain as against a normal resistor, typically used in a Gilbert cell mixer, in the topology also helps in breaking the tradeoff between gain and IR-drop induced headroom constraint. Two versions of this down-converter, one with common-gate input for broadband applications while another with a common-source input for narrowband applications, have been implemented. The common-source input version provides better sensitivity performance. A direct-conversion quadrature receiver with such a down-converter core and integrated dividers for I-Q generation has also been implemented. Measurement results from the above designs have been shown to validate the effectiveness of the circuit techniques and also the ability of the proposed architecture to provide for significant enhancement in the dynamic range per unit power dissipation, in comparison to prior state-of-the-art.

Oscillators with low phase noise are essential for reducing sensitivity degradation from reciprocal mixing, a problem which has been aggravated by to increasingly severe co-existence requirements arising from enhanced usage of available spectrum. A voltage controlled LC oscillator employing current-reuse amongst multiple capacitively coupled cores has been proposed to improve the power-efficiency over conventional implementations. Coupling of the cores results in AC power combining and can ensure both in-phase operation

as also reduction of phase noise while DC power is held unchanged through current reuse. Coupled oscillators, as the one proposed, open up the possibility of multi-mode oscillation. A detailed analysis of such mechanisms have been presented in the context of a widely used quadrature transistor-coupled oscillator. Cross-compression mechanism among competing modes have been discussed to explain how non-dominant modes are effectively suppressed as oscillation amplitude grows to reach steady state.

8.2 Future Work

The baseband linearization technique used in the proposed receiver down-converter operates over a narrow band of bias voltages about the optimum value required for cancellation of the $3^{\text{rd}}-$order coefficient of nonlinearity. The optimum value is a function of the process, temperature and power supply. Moreover, it is dependent on the VGA setting as implemented in the receiver. Consequently, an approach is required to set this bias voltage robustly across different PVT conditions and gain settings.

Although the dynamic range enhancement techniques have been introduced in the context of our bias-shared receiver down-converter, they are in general applicable to circuit elements of other radio architectures. Moreover, the bias-sharing arrangement can be potentially applied in transmitters too, e.g., in an up-converting driver stage for power amplifier, by suitable replacement of the passives with inductors. Such possible applications of the circuit techniques and the topology discussed can also be studied for enhancing power

efficiency of the designs. Emerging mm-wave applications can also potentially benefit from the use of such techniques, since power dissipation is a critical constraint in such designs.

Low phase noise VCOs, serving as the source circuit for the LO synthesis chain, typically have to drive large capacitive load presented by e.g., divider or mixer. Consequently, they are often buffered to minimize the impact of loading on oscillation frequency. To ensure minimization of performance degradation arising from reciprocal mixing, the additive noise from these stages, including noise from the supplies of the buffers, has to be minimized. Rigorous analysis of such phase noise degradation mechanisms are consequently required to derive specifications of the necessary circuit elements.

Often, wireless transceivers work across a time-variant communication channel which implies blockers may arise only intermittently. Consequently, to maximize the system energy efficiency, a time-multiplexed LO consisting of a low noise oscillator and a low power oscillator can be investigated. Alternatively, the design of a dynamically-biased oscillator that trades-off noise for power can be considered.

Appendices

Appendix A

Impedance Analysis of the Passive Mixer

We evaluate the impedance looking into the passive commutating mixer core driven in current mode by considering the ideal model shown in Fig. A.1. We assume the switching function is

$$p(t) = \frac{4}{\pi} \quad \sum_{n=1,3,..} \frac{\sin n\omega_{LO}t}{n} \tag{A.1}$$

and the input current is $i_{in} = I_0 \sin \omega_{in} t$

Using the annotation of Fig. (A.1) and the above expressions the baseband

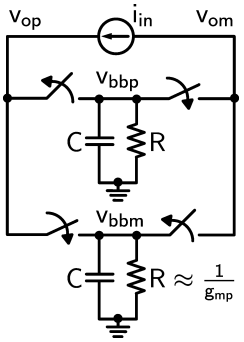


Figure A.1: Model for estimation of impedance looking into current mode passive mixer

output, v_{bbp}, can be shown as,

$$v_{bbp} = \frac{1}{C}\int_0^t (p(t)i - \frac{v_{bbp}}{R})\mathrm{d}t \approx \frac{2}{\pi}\frac{I_0}{C}\frac{\sin(\omega_{LO}-\omega_{in})t}{\omega_{LO}-\omega_{in}} - \frac{1}{RC}\int_0^t v_{bbp}\mathrm{d}t \quad \text{(A.2)}$$

Solving the above equation (A.2) we obtain,

$$v_{bbp} = \frac{2}{\pi}I_0\frac{R}{\sqrt{1+(\Delta\omega CR)^2}}\cos(\Delta\omega t + \arctan\Delta\omega CR) \quad \text{(A.3)}$$

where, $\Delta\omega = \omega_{LO} - \omega_{in}$.

From the equation (A.3) we get the voltage established at the current source terminals ($= v_{op} - v_{om}$),

$$v_o = 2p(t)v_{bbp} \approx \frac{8}{\pi^2}\frac{I_0 R}{\sqrt{1+(\Delta\omega CR)^2}}\sin(\omega_{in}t - \arctan\Delta\omega CR) \quad \text{(A.4)}$$

Thus we can conclude that for $\Delta\omega \to 0$, the impedance $Z_{in,mxr}(\omega_{in})$ looking into the passive mixer core is $\approx 8R/\pi^2$ for $\omega_{in} \approx \omega_{LO}$.

Appendix B

Non-linearity Analysis of the Baseband Amplifier

The baseband node voltages and branch currents due to excitation of transimpedance amplifier by i_{in} are shown in Fig. 3.8(b). Applying KVL we obtain,

$$v_x = v_{out} + i_{in}(R_{F0} + R_{F2}v_{out}^2) \tag{B.1}$$

Using KCL and the power series expansion for the non-linear transconductor we get,

$$i_{out} = a_1 v_x + a_2 v_x^2 + a_3 v_x^3 = i_{in} \tag{B.2}$$

We assume,

$$v_{out} = b_1 i_{in} + b_2 i_{in}^2 + b_3 i_{in}^3 \tag{B.3}$$

On substituting equations (B.1), (B.3) in (B.2) and ignoring the terms with order greater than 3 we obtain,

$$\begin{aligned} i_{in} = {} & a_1(b_1 + R_{F0})i_{in} + \{a_1 b_2 + a_2(b_1 + R_{F0})^2\}i_{in}^2 + \\ & \{a_1 b_3 + 2a_2(b_1 + R_{F0})b_2 + a_1 b_1^2 R_{F2} + a_3(b_1 + R_{F0})^3\}i_{in}^3 \end{aligned} \tag{B.4}$$

Equating the coefficients of identical powers of i_{in} in L.H.S. and R.H.S. of equation (B.4) we can derive the set of non-linear coefficients for the baseband amplifier.

Appendix C

Bias Parameters for the Squarer Circuit

To find the dependence of the non-linear coefficients for the feedback resistor on bias parameters, we first determine the gain of the squarer circuit ($G_{C,SQR}$). Assuming its transistors (M_{NSQR}), having $L \gg L_{min}$, are biased in saturation and are ideally square law devices $G_{C,SQR}$ can be derived as follows. The output voltage of the squarer is given by

$$v_{o,SQR} = (V_{SW} - \frac{k_n W_{SQR}}{L_{SQR}} V_{GST,SQR}^2 R_{NLC}) - \frac{k_n W_{SQR}}{L_{SQR}} R_{NLC} \beta^2 v_{out}^2 \qquad \text{(C.1)}$$

where v_{out} is the single-ended output of the mixer, $v_{o,SQR}$ is the squarer output, β is the voltage scaling factor from the output of the mixer to the input of the squarer, $k_n = \mu_n \varepsilon_{ox}/t_{ox}$, $V_{GST,SQR} = V_{GS,SQR}$ - $V_{T,SQR}$, W_{SQR}/L_{SQR} is the aspect ratio of M_{NSQR} and V_{SW} is the bias fed through R_{NLC}. This implies

$$G_{C,SQR} = \frac{k_n W_{SQR}}{L_{SQR}} R_{NLC} \beta^2 \qquad \text{(C.2)}$$

From Fig. 3.5 we can see that the total resistance in the feedback path for the transimpedance, which consists of a linear resistor R_{FL} in series with the

MOS resistor (M_{NRES}), is

$$R_{FL} + r_{SW} \approx R_{FL} + \frac{1}{k_n \frac{W_{SW}}{L_{SW}} v_{GST}} = R_{FL} + \frac{1}{k_n \frac{W_{SW}}{L_{SW}} (V_{GST} - G_{C,SQR} v_{out}^2)}$$
$$\approx R_{FL} + R_{SW} + \frac{G_{C,SQR} R_{SW}}{V_{GST}} v_{out}^2 \quad \text{(C.3)}$$

Here, $r_{SW} = v_{DS,SW}/i_{DS,SW}$, W_{SW}/L_{SW} is the aspect ratio of M_{NRES} and

$$V_{GST} = V_{GS,SW} - V_{T,SW} = V_{SW} - \frac{k_n W_{SQR}}{L_{SQR}} V_{GST,SQR}^2 R_{NLC} - (V_{BIAS} - I_{R_{bias}} R_{bias}) - V_{T,SW} \quad \text{(C.4)}$$

Appendix D

Non-linear Coefficients of the Reactively Degenerated Coupling-path Transistors

The dependence of coupling transistor output current on the differential input voltage, from Fig. 7.2, can be expressed as,

$$i_p(v_x) = f(v_{gsp}) = a_{1d}v_{gsp} + a_{2d}v_{gsp}^2 + a_{3d}v_{gsp}^3 \tag{D.1}$$

Representing the gate-source voltage and output current as the following Volterra series in terms of the input voltage v_x,

$$v_{gsp} = B_1(s)\circ v_x + B_2(s_1,s_2)\circ v_x^2 + B_3(s_1,s_2,s_3)\circ v_x^3 \tag{D.2}$$

$$i_p(v_x) = C_1(s)\circ v_x + C_2(s_1,s_2)\circ v_x^2 + C_3(s_1,s_2,s_3)\circ v_x^3 \tag{D.3}$$

and solving for the coefficients, we get,

$$B_1(s) = \frac{1}{2}\frac{1}{1 + a_{1d}Z_d(s) + sC_{gs}Z_d(s)} \tag{D.4}$$

$$B_2(s_1,s_2) = -\frac{2a_{2d}Z_d(s_1+s_2)B_1(s_1)B_1(s_2)B_1(s_1+s_2)}{1 - 2B_1(s_1+s_2)} \tag{D.5}$$

$$\begin{aligned} B_3(s_1,s_2,s_3) = {} & -2Z_d(s_1+s_2+s_3)B_1(s_1+s_2+s_3) \\ & (2a_{2d}\overline{B_1(s_1)B_2(s_2,s_3)} + a_{3d}B_1(s_1)B_1(s_2)B_1(s_3)) \end{aligned} \tag{D.6}$$

The relationships between B_i and C_i are given by

$$C_1(s) = a_{1d}B_1(s) \tag{D.7}$$

$$C_2(s_1,s_2) = a_{1d}B_2(s_1,s_2) + a_{2d}B_1(s_1)B_1(s_2) \tag{D.8}$$

$$\begin{aligned} C_3(s_1,s_2,s_3) = {} & a_{1d}B_3(s_1,s_2,s_3) + 2a_{2d}\overline{B_1(s_1)B_2(s_2,s_3)} \\ & + a_{3d}B_1(s_1)B_1(s_2)B_1(s_3) \end{aligned} \tag{D.9}$$

Due to differential symmetry the differential voltage across the load is related to $C_1(s)$ and $C_3(s_1, s_2, s_3)$. We ignore the frequency dependence of $C_1(s)$ and $C_3(s_1, s_2, s_3)$ and approximate them with the values evaluated at ω_r. Using this approximation in (D.7) and (D.9) we obtain

$$C_1(s_r) = a_{1d} B_1(s_r) = \frac{1}{2} \frac{a_{1d}}{1 + a_{1d} Z_d(s_r) + s_r C_{gs} Z_d(s_r)} \tag{D.10}$$

$$\begin{aligned} C_3(s_r, s_r, -s_r) = {} & B_1(s_r) |B_1(s_r)|^2 (1 - 2 a_{1d} Z_d(s_r) B_1(s_r)) \\ & (a_{3d} - \frac{4 a_{2d}^2}{3} \frac{Z_d(2 s_r) B_1(2 s_r)}{1 - 2 B_1(2 s_r)} - \frac{4 a_{2d}^2}{3 a_{1d}}) \end{aligned} \tag{D.11}$$

For $|s_r C_{gs}| \ll a_{1d}$,

$$\angle C_1(s_r) = -\gamma = -\mathrm{sgn}(\angle Z_d(s_r)) \tan^{-1}(a_{1d} |Z_d(s_r)|) \tag{D.12}$$

$$\boldsymbol{a_{1c}} = C_1(s_r) = \frac{1}{2} \frac{a_{1d}}{1 + a_{1d} Z_d(s_r)} \tag{D.13}$$

Appendix E

Solution of System Differential Equations for the Quadrature Oscillator

Using the quasiharmonic approximations [67], from equation (7.3),

$$\dot{v_1} = -\alpha_1\omega_1 \sin\theta_1 + \alpha_2\omega_2 \cos\theta_2 \tag{E.1a}$$
$$\dot{v_2} = \quad \alpha_1\omega_1 \cos\theta_1 - \alpha_2\omega_2 \sin\theta_2 \tag{E.1b}$$

Taking time derivatives of (7.3) and using (E.1) we get,

$$\dot{\alpha_1}\cos\theta_1 + \dot{\alpha_2}\sin\theta_2 = \quad \alpha_1\dot{\phi_1}\sin\theta_1 - \alpha_2\dot{\phi_2}\cos\theta_2 \tag{E.2}$$
$$\dot{\alpha_1}\sin\theta_1 + \dot{\alpha_2}\cos\theta_2 = -\alpha_1\dot{\phi_1}\cos\theta_1 + \alpha_2\dot{\phi_2}\sin\theta_2 \tag{E.3}$$

Employing equations (7.2), (7.3), (E.1) and its derivative, the system equations are transformed into relations in $\{\alpha,\ \phi\}$. The resulting equation set consists of (E.2), (E.3) and

$$\begin{aligned} -\omega_1\dot{\alpha_1}\sin\theta_1 - \omega_1\alpha_1\dot{\phi_1}\cos\theta_1 + \omega_2\dot{\alpha_2}\cos\theta_2 & \\ -\omega_2\alpha_2\dot{\phi_2}\sin\theta_2 &= F_1 \end{aligned} \tag{E.4}$$

$$\begin{aligned} \omega_1\dot{\alpha_1}\cos\theta_1 - \omega_1\alpha_1\dot{\phi_1}\sin\theta_1 - \omega_2\dot{\alpha_2}\sin\theta_2 & \\ -\omega_2\alpha_2\dot{\phi_2}\cos\theta_2 &= F_2 \end{aligned} \tag{E.5}$$

where,

$$\begin{aligned} F_1 = -\frac{1}{C}\dot{v_1}(G - a_1 - 3a_3v_1^2) + \frac{1}{C}\frac{\mathrm{d}}{\mathrm{d}t}(C_1(\omega)\circ v_2 + \\ C_3(\omega_a,\omega_b,\omega_c)\circ v_2^3) + (\omega_1^2 - \frac{1}{LC})\alpha_1\cos\theta_1 + \end{aligned}$$

$$(\omega_2^2 - \frac{1}{LC})\alpha_2 \sin\theta_2 \tag{E.6}$$

$$F_2 = -\frac{1}{C}\dot{v}_2(G - a_1 - 3a_3 v_2^2) - \frac{1}{C}\frac{\mathrm{d}}{\mathrm{d}t}(C_1(\omega) \circ v_1 + C_3(\omega_a, \omega_b, \omega_c) \circ v_1^3) + (\omega_1^2 - \frac{1}{LC})\alpha_1 \sin\theta_1 + (\omega_2^2 - \frac{1}{LC})\alpha_2 \cos\theta_2 \tag{E.7}$$

Assuming quasiharmonic behavior in F_1 and F_2 and using the Method of First Approximation for derivatives of α, ϕ we get the final autonomous state equations given by (7.5). While applying First Approximation, the averaging interval is assumed to be large enough so that the slowest non-DC beat product terms with frequency $(\omega_2 - \omega_1)/2\pi$ are averaged out. The objective of this constraint is to smooth out all high frequency variations in time derivatives of α and ϕ as in original formulation of Kryloff.

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This dissertation was typeset with LaTeX[†] by the author.

[†]LaTeX is a document preparation system developed by Leslie Lamport as a special version of Donald Knuth's TeX Program.